

Datasheet

AP6212A

IEEE 802.11b/g/n 1x1

WiFi with Bluetooth5.2 Combo Sip Module

Contents

1. Introduction.....	3
1.1 Product Overview	3
1.2 Product Feature.....	3
1.2.1 WLAN.....	3
1.2.2 Bluetooth.....	3
2. Specification	4
2.1 General Specification	4
2.2 WiFi 2.4GHz RF Specification	5
2.3 Bluetooth RF Specification	6
3. Electrical Characteristics	7
3.1 Absolute Maximum Ratings	7
3.2 Recommended Operating Rating	7
4. Host Interface Timing Diagram.....	8
4.1 Power-up Sequence Timing Diagram.....	8
4.2 SDIO Default Mode Timing Diagram.....	10
4.3 SDIO High Speed Mode Timing Diagram.....	11
5. Power Consumption	12
6. Block Diagram.....	13
7. Pin Definition.....	14
7.1 Pin Map.....	14
7.2 Pin Definition	14
8. Mechanical Specification	16
8.1 Module Dimension	16
8.2 PCB Footprint.....	17
9. External Clock Reference	18
9.1 SDIO Interface Description	19
10. Recommended Reflow Profile	20
10.1 Caution for SMT Preparation	21
11. Package Information.....	22
12. Ordering Information.....	25

1. Introduction

1.1 Product Overview

AP6212A is 11b/g/n 1T1R WiFi +Bluetooth 5.2 WiFi module. It's a highly integrated single-chip solution and provides the highest level of integration for a mobile or handheld wireless system. offers the low-cost in the industry for smartphones, tablets, and a wide range of other portable devices. The WiFi module is designed to address the needs of highly mobile devices that require minimal power consumption and compact size. It implements the world's most advanced Enhanced Collaborative Coexistence algorithms and hardware mechanisms, allowing for an extremely collaborative WLAN and Bluetooth coexistence.

It can achieve up to a speed of 72.2Mbps with single stream in 802.11n draft, 54Mbps as specified in IEEE 802.11g, or 11Mbps for IEEE 802.11b to connect to the wireless LAN. The integrated module provides SDIO interface for WiFi, UART / I2S / PCM interface for Bluetooth.

This compact module is a total solution for a combination of WiFi + BT technologies. The module is specifically developed for Smart phones and Portable devices.

1.2 Product Feature

1.2.1 WLAN

- Single-band 2.4GHz IEEE 802.11b/g/n
- Supports standard interfaces SDIO v2.0(50MHz, 4-bit and 1-bit)
- Simultaneous BT/WLAN receive with single antenna
- Concurrent Bluetooth and WLAN operation
- IEEE Co-existence technologies are integrated die solution

1.2.2 Bluetooth

- BT host digital interface:
 - UART (up to 4 Mbps)
- Bluetooth V5.2 with integrated Class 1.5 PA and Low Energy (BLE) support.
- ECI — enhanced coexistence support, ability to coordinate BT SCO transmissions around WLAN receives

2. Specification

2.1 General Specification

Standards	IEEE 802.11b/g/n WiFi+BT4.1 Module Bluetooth V5.2, V5.0, V4.2, V4.1, V4.0 LE, V3.0+HS, V2.1+EDR
Chipset	Synaptics
Operating Frequency	2.400 GHz ~ 2.4835 GHz (2.4GHz ISM Band) Bluetooth: 2.402 GHz ~ 2.480 GHz
Modulation	WiFi: 802.11b: DSSS (DBPSK, DQPSK, CCK) 802.11g: OFDM (BPSK, QPSK, 16-QAM, 64-QAM) 802.11gn: OFDM (BPSK, QPSK, 16-QAM, 64-QAM) BT: GFSK, $\pi/4$ -DQPSK, 8-DPSK
Interface	WLAN: SDIO 2.0 Bluetooth: UART / PCM
Form Factor	Stamp Type
Antenna	External
Dimension	L x W x H: 12 x 12 x 1.5 (typical) mm
Operating temperature	-30°C~85°C
Storage temperature	-40°C~85°C
Humidity (Non-Condensing)	Operation : 10% to 95% Storage : 5% to 95%
Weight	0.45g
Driver Support	Linux, Android

Note: a. The operating temperature 65 to 85°C is feasible at conditional environment. Please examine the reliability on final product.

b. Functionality is guaranteed across this range of temperature. Optimal RF performance as specified in the data sheet, however, is guaranteed only for -10°C to 55°C and 3.2V < VBAT < 3.8V.

2.2 WiFi 2.4GHz RF Specification

Conditions: VBAT=3.3V; VDDIO=3.3V; Temp:25°C

Output Power	802.11b /11Mbps : 16 dBm ± 1.5 dB @ EVM ≤ -9dB	
	802.11g /54Mbps : 15 dBm ± 1.5 dB @ EVM ≤ -25dB	
	802.11n /65Mbps : 14 dBm ± 1.5 dB @ EVM ≤ -27dB	
Sensitivity, tolerance ± 2 dB		
CCK modulation PER ≤ 8% 、 OFDM modulation PER ≤ 10%		
802.11n,20MHz	- MCS=0	PER @ -88 dBm, ± 2 dB
	- MCS=1	PER @ -87 dBm, ± 2 dB
	- MCS=2	PER @ -86 dBm, ± 2 dB
	- MCS=3	PER @ -84 dBm, ± 2 dB
	- MCS=4	PER @ -77 dBm, ± 2 dB
	- MCS=5	PER @ -75 dBm, ± 2 dB
	- MCS=6	PER @ -72 dBm, ± 2 dB
	- MCS=7	PER @ -68 dBm, ± 2 dB
802.11g	- 6Mbps	PER @ -90 dBm, ± 2 dB
	- 9Mbps	PER @ -90 dBm, ± 2 dB
	- 12Mbps	PER @ -88 dBm, ± 2 dB
	- 18Mbps	PER @ -86 dBm, ± 2 dB
	- 24Mbps	PER @ -83 dBm, ± 2 dB
	- 36Mbps	PER @ -80 dBm, ± 2 dB
	- 48Mbps	PER @ -77 dBm, ± 2 dB
	- 54Mbps	PER @ -75 dBm, ± 2 dB
802.11b	- 1Mbps	PER @ -95 dBm, ± 2 dB
	- 2Mbps	PER @ -94 dBm, ± 2 dB
	- 5.5Mbps	PER @ -92 dBm, ± 2 dB
	- 11Mbps	PER @ -88 dBm, ± 2 dB
Data Rate	802.11b : 1, 2, 5.5, 11Mbps	
	802.11g : 6, 9, 12, 18, 24, 36, 48, 54Mbps	
Data Rate (20MHz ,Long GI,800ns)	802.11n: 6.5, 13, 19.5, 26, 39, 52, 58.5, 65Mbps	
Data Rate (20MHz ,short GI,400ns)	802.11n : 7.2, 14.4, 21.7, 28.9, 43.3, 57.8, 65,72.2Mbps	
Maximum Input Level	802.11b : -10 dBm	
	802.11g/n : -20 dBm	

Antenna Reference	Small antennas with 0~2 dBi peak gain
-------------------	---------------------------------------

2.3 Bluetooth RF Specification

Conditions: VBAT=3.3V ; VDDIO=3.3V ; Temp:25°C

RF Specification			
	Min	Typical	Max
Output Power*	0	5	10
Sensitivity @ BER=0.1% for GFSK (1Mbps)		-86 dBm	
Sensitivity @ BER=0.01% for $\pi/4$ -DQPSK (2Mbps)		-87 dBm	
Sensitivity @ BER=0.01% for 8DPSK (3Mbps)		-85 dBm	
Sensitivity @ PER=30.8% for LE		-86 dBm	
Maximum Input Level	GFSK (1Mbps):-20dBm		
	$\pi/4$ -DQPSK (2Mbps) :-20dBm		
	8DPSK (3Mbps) :-20dBm		

Note* : The Bluetooth output power is able to be configured by firmware (hcd file).

3. Electrical Characteristics

3.1 Absolute Maximum Ratings

Symbol	Description	Min.	Max.	Unit
VBAT	Input supply Voltage	-0.5	+5.25	V
VDDIO	Digital/Bluetooth/SDIO/ I/O Voltage	-0.5	+3.8	V

3.2 Recommended Operating Rating

The module requires two power supplies: VBAT and VDDIO.

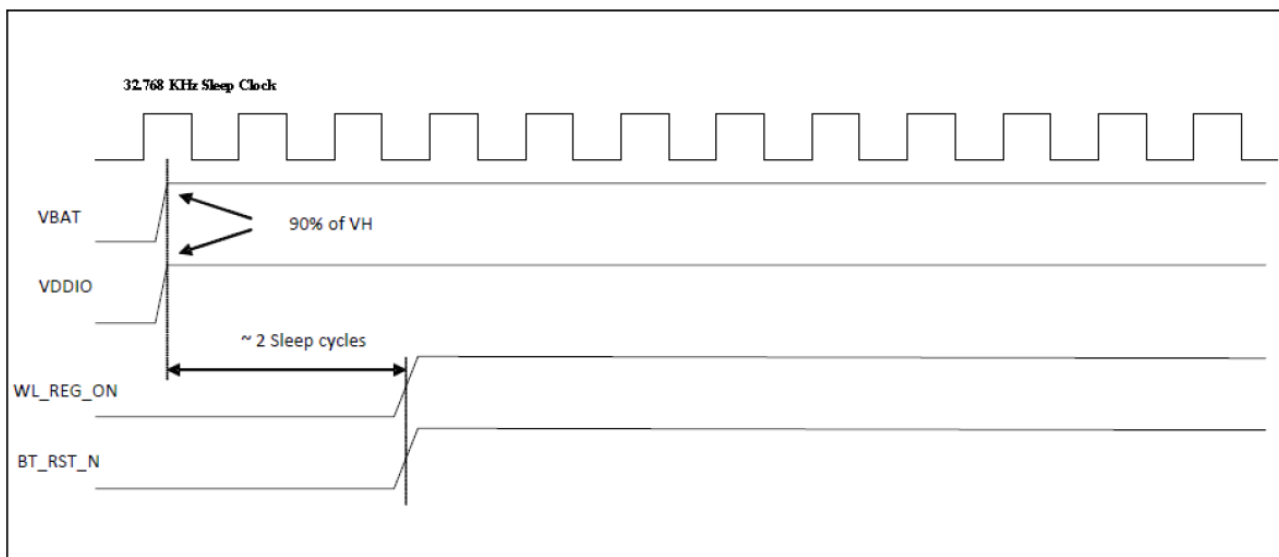
Voltage rails	Min.	Typ.	Max.	Unit
Operating Temperature	-30	25	85	deg.C
VBAT	3.0	3.3	3.8	V
VDDIO	1.71	1.8	1.98	V
	2.97	3.3	3.63	V

4. Host Interface Timing Diagram

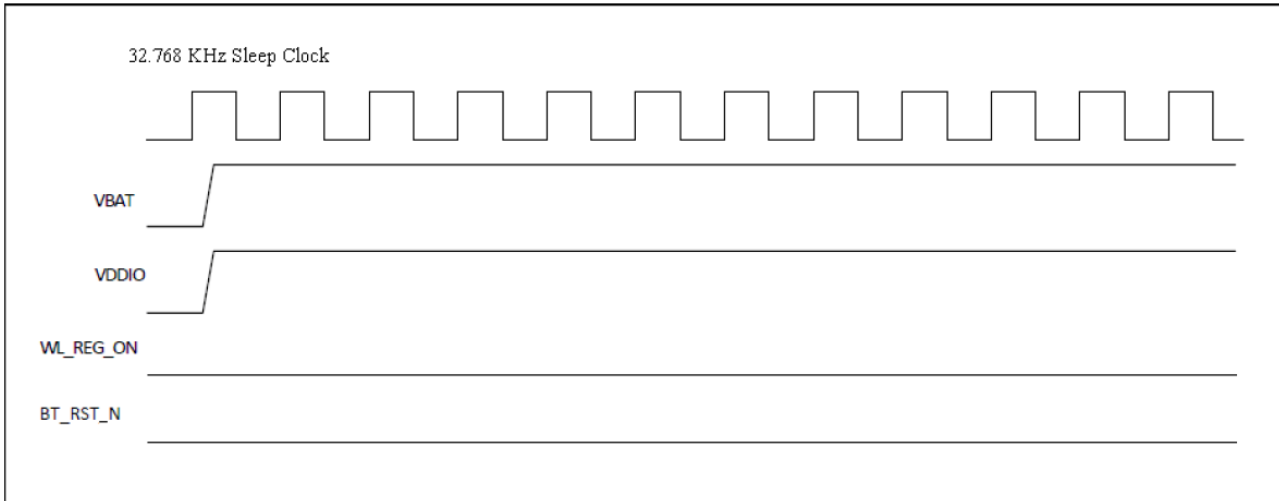
4.1 Power-up Sequence Timing Diagram

The module has signals that allow the host to control power consumption by enabling or disabling the Bluetooth, WLAN and internal regulator blocks. These signals are described below. Additionally, diagrams are provided to indicate proper sequencing of the signals for various operating states. The timing values indicated are minimum required values; longer delays are also acceptable.

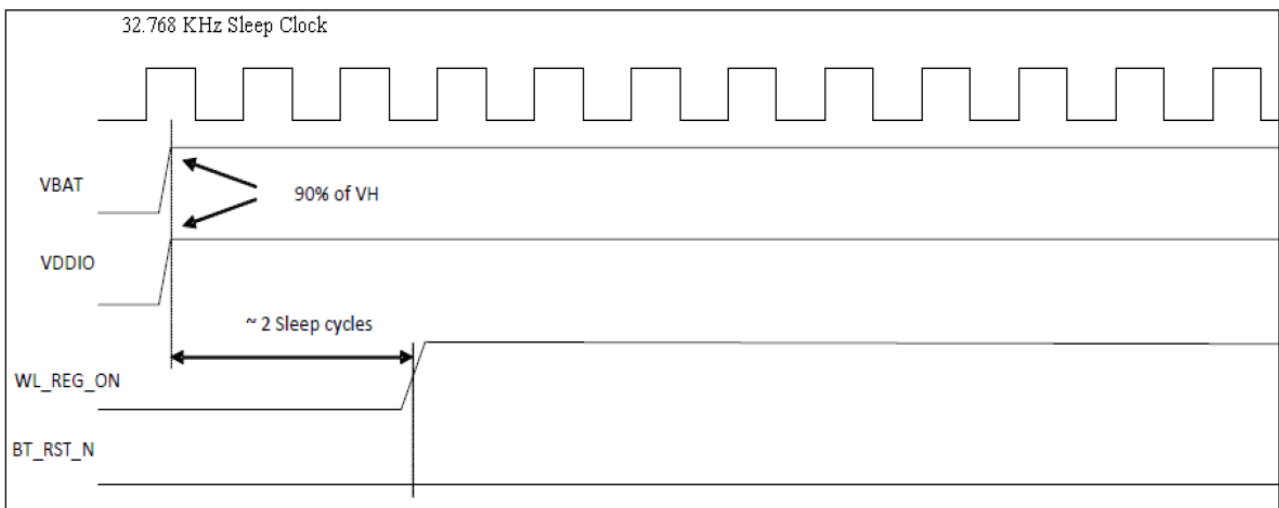
- **WL_REG_ON**: Used by the PMU to power up the WLAN section. When this pin is high, the regulators are enabled and the WLAN section is out of reset. When this pin is low the WLAN section is in reset.
- **BT_RST_N**: Low asserting reset for Bluetooth. This pin has no effect on WLAN and does not control any PMU functions. This pin must be driven high or low (not left floating).



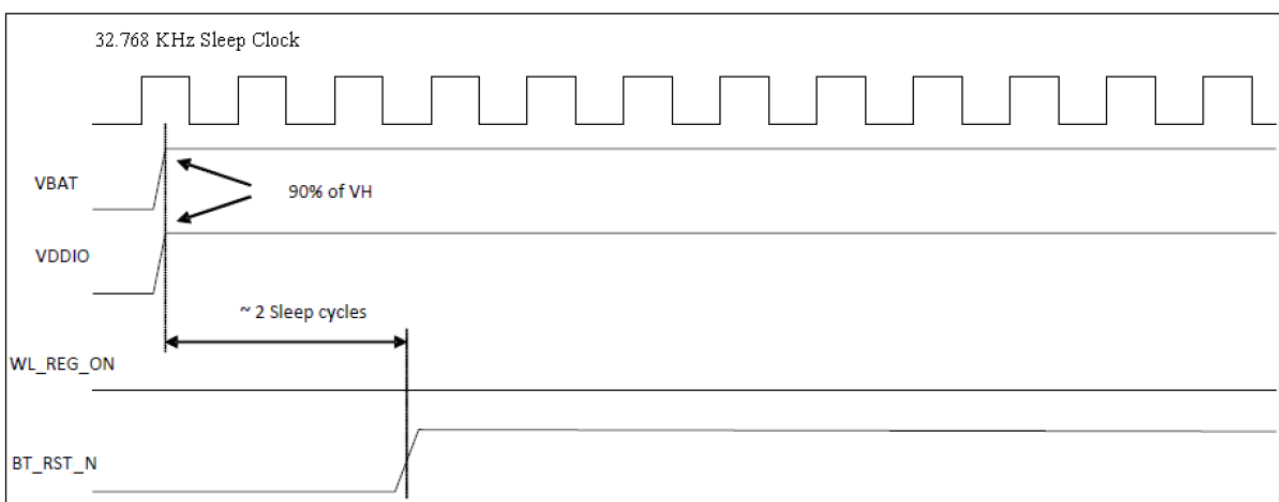
WLAN=ON, Bluetooth=ON



WLAN=OFF, Bluetooth=OFF

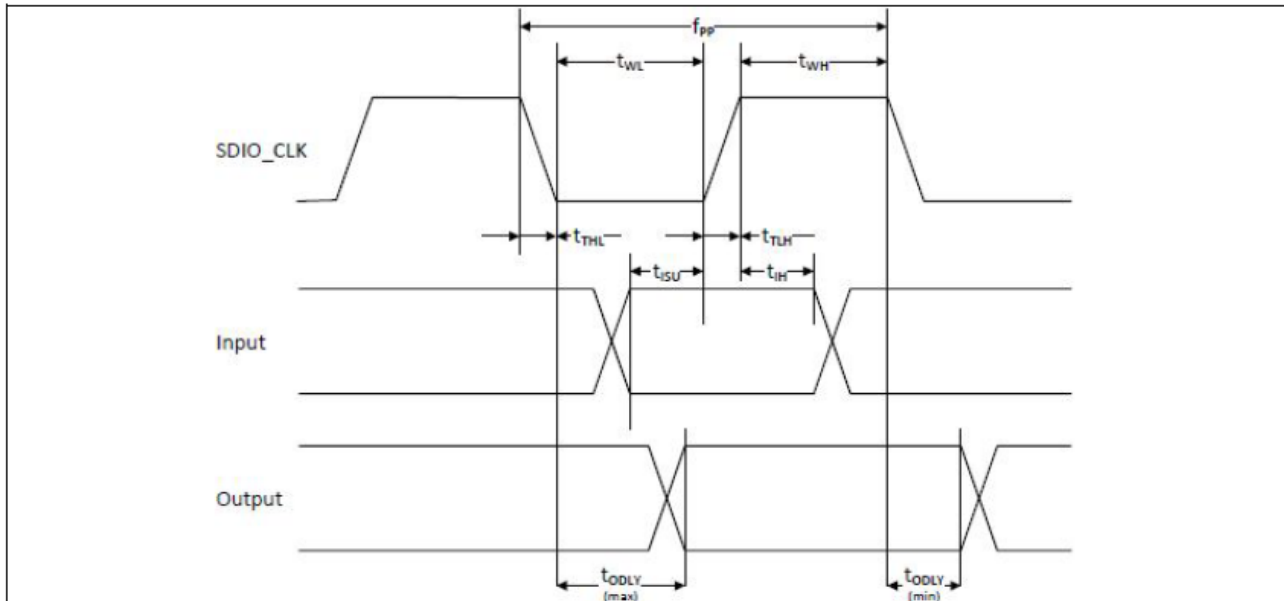


WLAN=ON, Bluetooth=OFF



WLAN=OFF, Bluetooth=ON

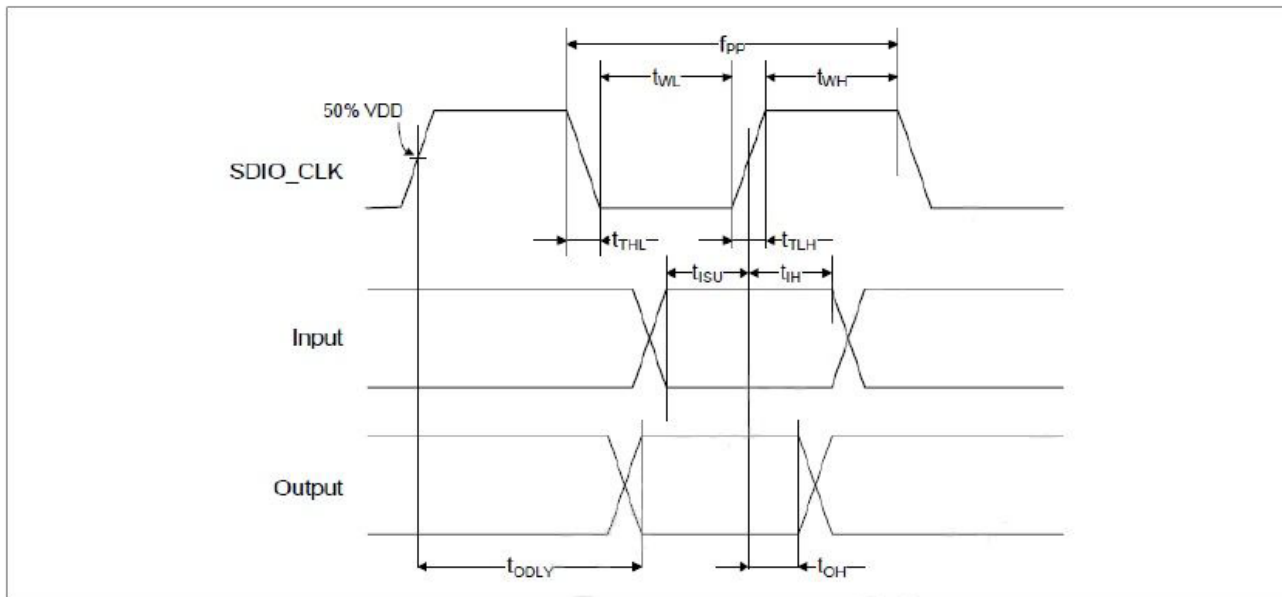
4.2 SDIO Default Mode Timing Diagram



Parameter	Symbol	Minimum	Typical	Maximum	Unit
SDIO CLK (ALL values are referred to minimum VIH and maximum VIL^b)					
Frequency – Data Transfer mode	fPP	0	-	25	MHz
Frequency – Identification mode	fOD	0	-	400	kHz
Clock low time	tWL	10	-	-	ns
Clock high time	tWH	10	-	-	ns
Clock rise time	tTlH	-	-	10	ns
Clock low time	tTHL	-	-	10	ns
Inputs : CMD, DAT(referenced to CLK)					
Input setup time	tISU	5	-	-	ns
Input hold time	tIH	5	-	-	ns
Outputs : CMD, DAT(referenced to CLK)					
Output delay time - Data Transfer mode	tODLY	0	-	14	ns
Output delay time - Identification mode	tODLY	0	-	50	ns

- Timing is based on $CL \leq 40$ pF load on CMD and Data.
- Min. (Vih) = $0.7 \times VDDIO$ and max. (Vil) = $0.2 \times VDDIO$

4.3 SDIO High Speed Mode Timing Diagram



Parameter	Symbol	Minimum	Typical	Maximum	Unit
SDIO CLK (ALL values are referred to minimum VIH and maximum VIL^b)					
Frequency – Data Transfer mode	f _{PP}	0	-	50	MHz
Frequency – Identification mode	f _{OD}	0	-	400	kHz
Clock low time	t _{WL}	7	-	-	ns
Clock high time	t _{WH}	7	-	-	ns
Clock rise time	t _{TLH}	-	-	3	ns
Clock low time	t _{THL}	-	-	3	ns
Inputs : CMD, DAT(referenced to CLK)					
Input setup time	t _{ISU}	6	-	-	ns
Input hold time	t _{IH}	2	-	-	ns
Outputs : CMD, DAT(referenced to CLK)					
Output delay time - Data Transfer mode	t _{ODLY}	-	-	14	ns
Output hold time	t _{OH}	2.5	-	-	ns
Total system capacitance(each line)	CL			40	pF

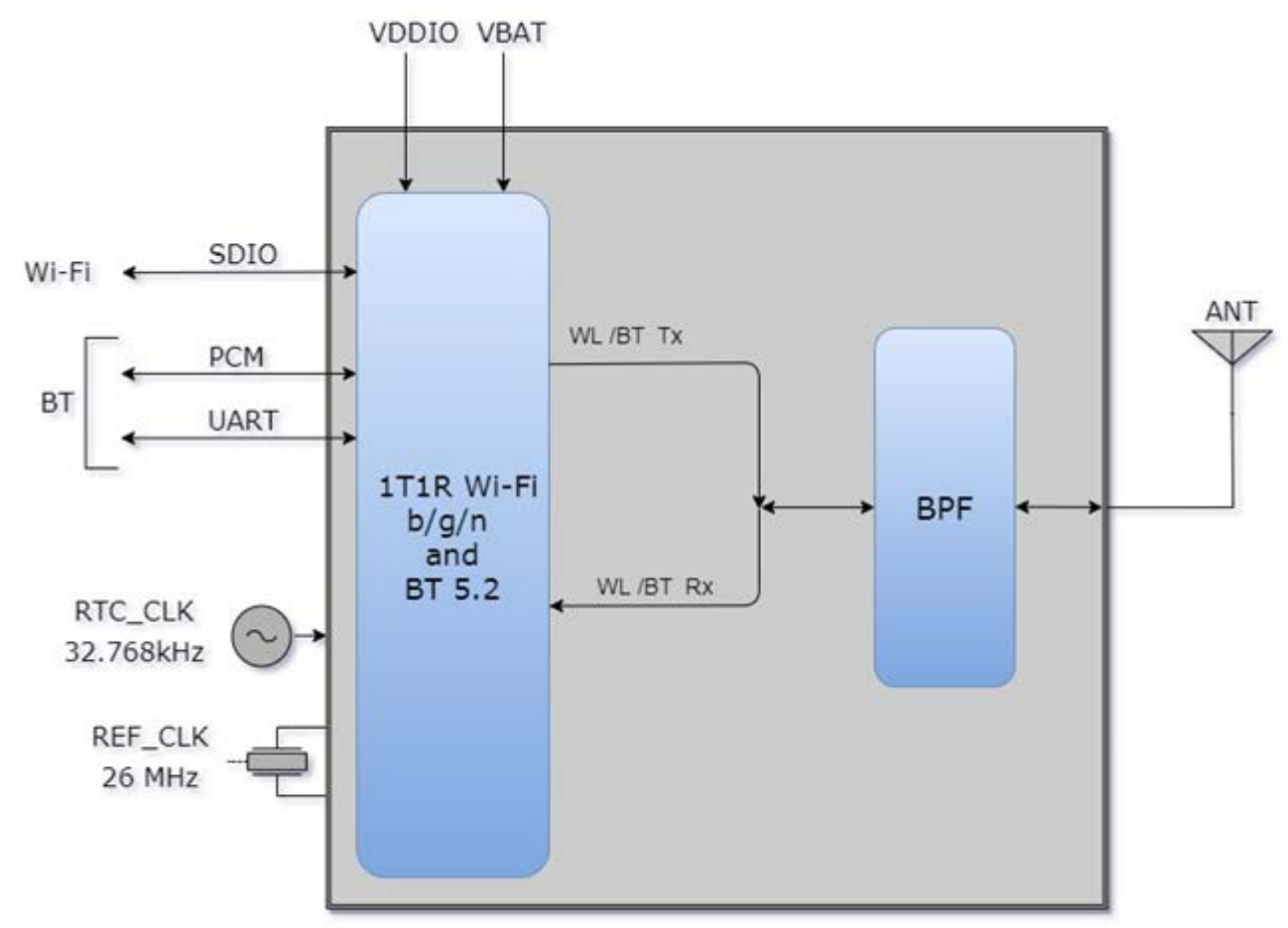
- a. Timing is based on CL ≤ 40pF load on CMD and Data.
- b. Min(V_{ih}) = 0.7 x V_{DDIO} and max(V_{il}) = 0.2 x V_{DDIO}

5. Power Consumption

■ 2.4 GHz

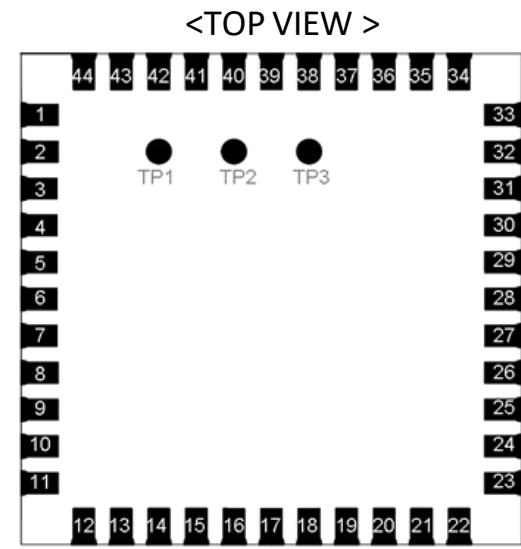
Test Mode	DUT Status	Supply Voltage (VBAT)	Supply Voltage (VDDIO)
802.11b mode	Continue TX	278.7mA	167.8uA
	Continue RX	42.1mA	87.1uA
802.11g mode	Continue TX	199.8mA	168.2uA
	Continue RX	42.1mA	87.1uA
802.11n mode	Continue TX	186.3mA	168.4uA
	Continue RX	41.3mA	86.9uA
Bluetooth mode	Continue TX	38.7mA	22.9uA
	Continue RX	22.1mA	22.9uA

6. Block Diagram



7. Pin Definition

7.1 Pin Map



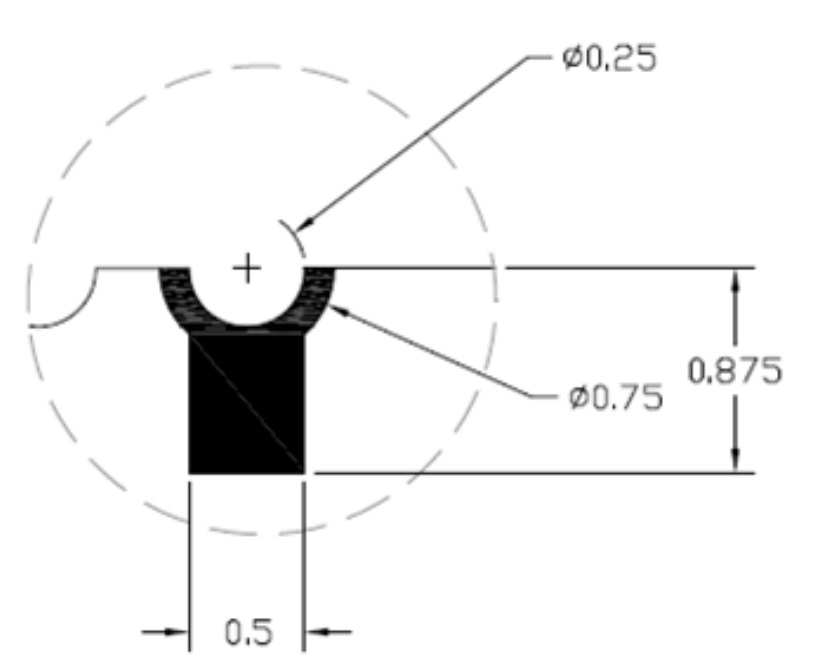
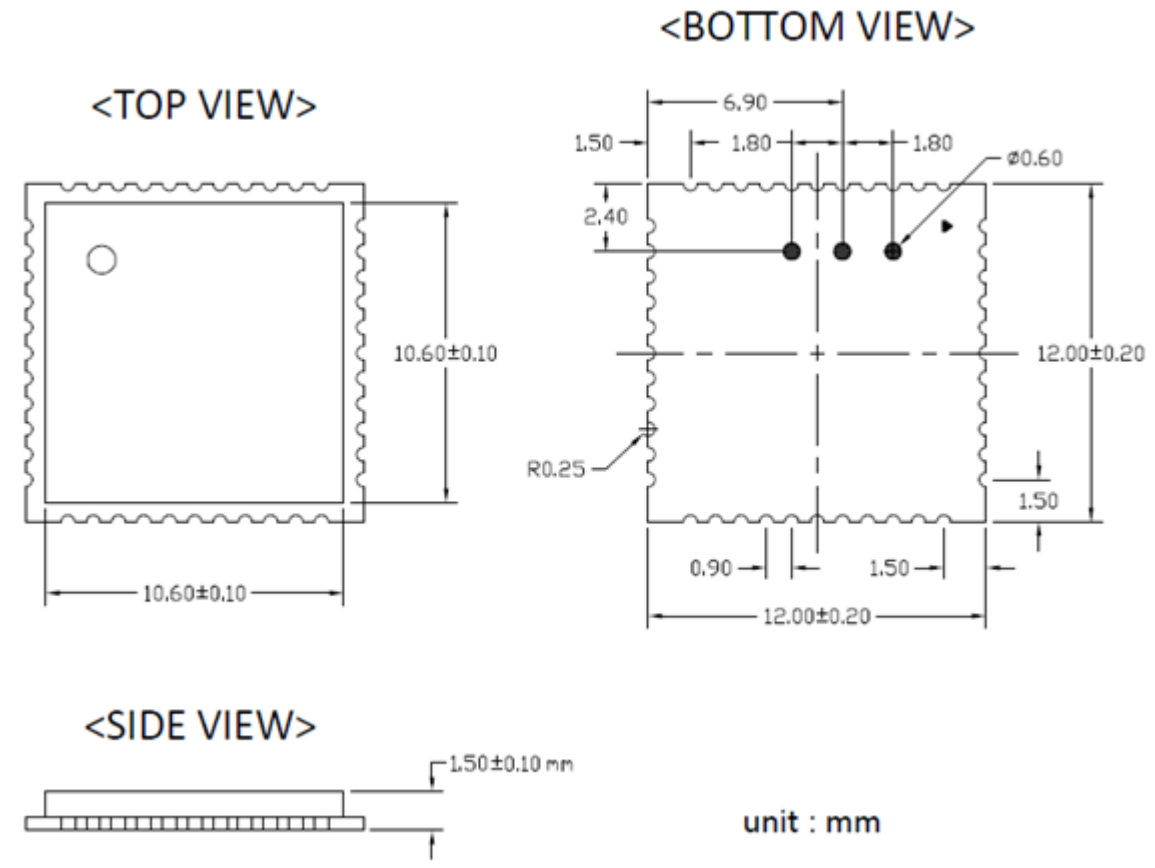
7.2 Pin Definition

NO	Name	Type	Description
1	GND	—	Ground connections
2	WL_BT_ANT	I/O	RF I/O port
3	GND	—	Ground connections
4	FM_RX	I	FM radio RF input antenna port
5	NC	—	Floating (Don't connected to ground)
6	BT_WAKE	I	HOST wake-up Bluetooth device
7	BT_HOST_WAKE	O	Bluetooth device to wake-up HOST
8	CLK_REQ	O	The AP6212A assert CLK_REQ when Bluetooth, or WLAN directs the host to turn on the reference clock. The CLK_REQ polarity is active-high. Add an external 100 kΩ pull-down resistor to ensure the signal is deasserted when the AP6212A powers up or resets when VDDIO is present.
9	VBAT	P	Main power voltage source input
10	XTAL_IN	I	Crystal input
11	XTAL_OUT	O	Crystal output
12	WL_REG_ON	I	Internal regulators power enable/disable

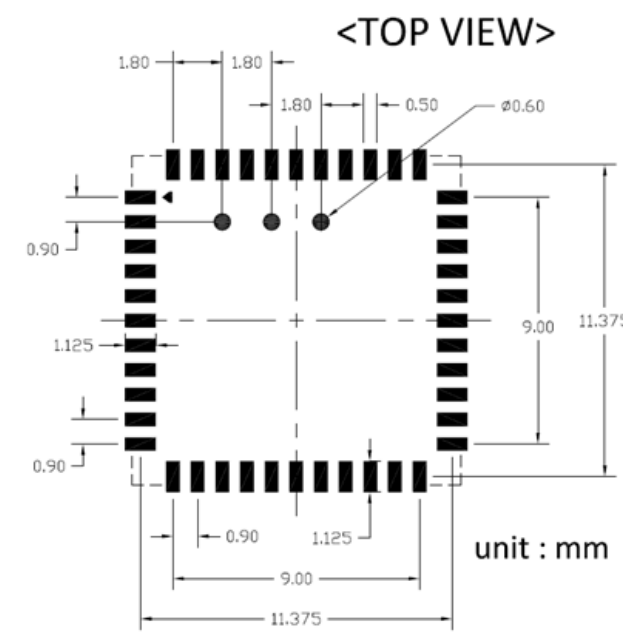
13	WL_HOST_WAKE	O	WLAN to wake-up HOST
14	SDIO_DATA_2	I/O	SDIO data line 2
15	SDIO_DATA_3	I/O	SDIO data line 3
16	SDIO_DATA_CMD	I/O	SDIO command line
17	SDIO_DATA_CLK	I/O	SDIO clock line
18	SDIO_DATA_0	I/O	SDIO data line 0
19	SDIO_DATA_1	I/O	SDIO data line 1
20	GND	—	Ground connections
21	VIN_LDO_OUT	P	Internal Buck voltage generation pin
22	VDDIO	P	I/O Voltage supply input
23	VIN_LDO	P	Internal Buck voltage generation pin
24	LPO	I	External Low Power Clock input (32.768KHz)
25	PCM_OUT	O	PCM Data output
26	PCM_CLK	I/O	PCM clock
27	PCM_IN	I	PCM data input
28	PCM_SYNC	I/O	PCM sync signal
29	NC	—	Floating (Don't connected to ground)
30	NC	—	Floating (Don't connected to ground)
31	GND	—	Ground connections
32	NC	—	Floating (Don't connected to ground)
33	GND	—	Ground connections
34	BT_RST_N	I	Low asserting reset for Bluetooth core
35	NC	—	Floating (Don't connected to ground)
36	GND	—	Ground connections
37	NC	—	Floating (Don't connected to ground)
38	NC	—	WL_GPIO2
39	GPIO2	I/O	WL_GPIO1
40	GPIO1	I/O	WiFi Co-existence pin with LTE
41	UART_RTS_N	O	Bluetooth/FM UART interface
42	UART_TXD	O	Bluetooth/FM UART interface
43	UART_RXD	I	Bluetooth/FM UART interface
44	UART_CTS_N	I	Bluetooth/FM UART interface
45	TP1	O	FM Analog AUDIO left output
46	TP2	O	FM Analog AUDIO right output
47	TP3 (NC)	—	Floating (Don't connected to ground)

8. Mechanical Specification

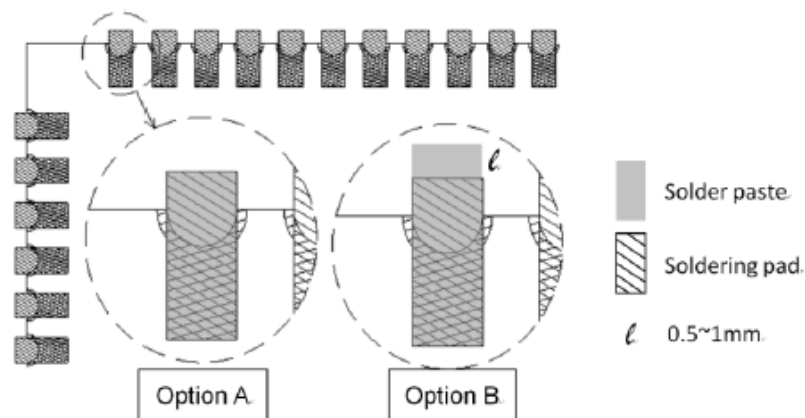
8.1 Module Dimension



8.2 PCB Footprint



- Solder paste layer design is generally the same as recommended footprint.
(錫膏層設計通常建議和焊墊尺寸相同)
- If soldering quality with good wetting on upright side is essential for PQC, how to optimize the aperture design in the stencil to adjust the amount of solder paste would be crucial.
In addition, a kind of stencil design with stepped thickness in partial area would be considered if the thickness of stencil is about 0.1mm or thinner. Please optimize the stencil design by manufacture engineer or contact SparkLAN FAE for assistance.
(如果模組吃錫品質考量側面爬錫，如何優化鋼網開孔設計以調整適當的錫膏量是非常重要的。尤其鋼網的厚度大約是 0.1mm或更薄時，可考慮局部加厚鋼網的設計。請諮詢製程工程師以優化鋼網的設計,或是聯絡速連通訊技術支持團隊).



9. External Clock Reference

External LPO signal characteristics

Parameter	Specification	Units
Nominal input frequency	32.768	kHz
Frequency accuracy	+/-30	ppm
Duty cycle	30 - 70	%
Module input Signal Level	400 ~ 3300	mV, p-p
Signal type	Square-wave	-
Input impedance	>100k <5	Ω pF
Clock jitter (integrated over 300Hz – 15KHz)	<1	Hz

External Ref_CLK signal characteristics

NO	Item	Symb.	Electrical Specification				Remark
			Min	Type	Max	Units	
1	Nominal Frequency	F0	26.00000			MHz	
2	Mode of Vibration		Fundamental				
3	Frequency Tolerance	$\Delta F/F0$	-10	-	10	ppm	at 25°C±3°C
4	Operating Temperature Range	T _{OPR}	-30	-	85	°C	
5	Frequency Stability	TC	-10	-	10	ppm	
6	Storage Temperature	T _{STG}	-55	-	125	°C	
7	Load capacitance	CL	-	16		pF	
8	Equivalent Series Resistance	ESR	-	-	50	Ω	
9	Drive Level	DL	-	100	200	uW	
10	Insulation Resistance	IR	500	-	-	M Ω	at 100V _{DC}
11	Shunt Capacitance	C0	-	-	3	pF	
12	Aging Per Year	Fa	-2	-	2	ppm	First Year

9.1 SDIO Interface Description

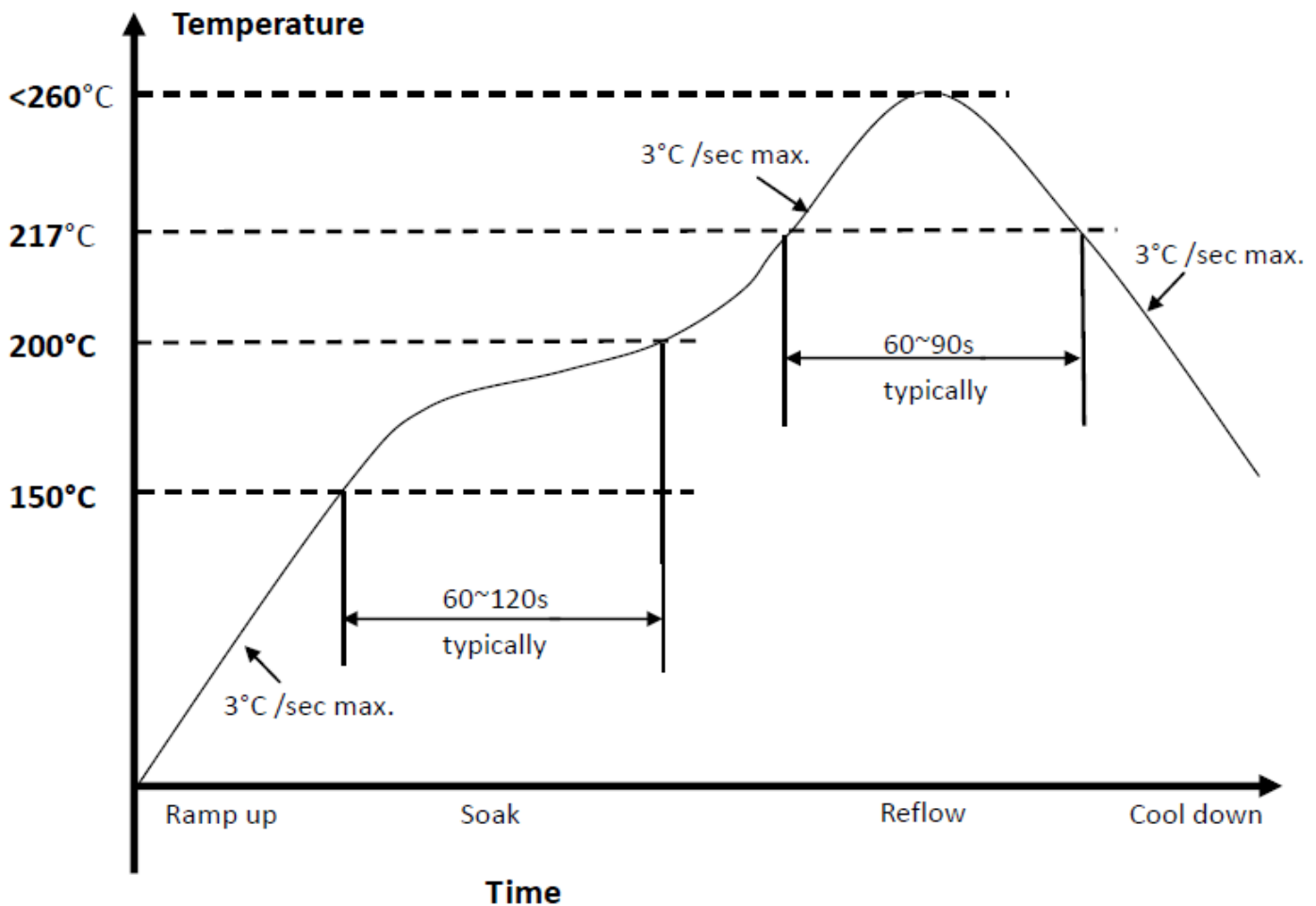
The module supports SDIO version 2.0 for 4-bit modes (100 Mbps), and high speed 4-bit (50 MHz clocks – 200 Mbps). It has the ability to stop the SDIO clock and map the interrupt signal into a GPIO pin. This ‘out-of-band’ interrupt signal notifies the host when the WLAN device wants to turn on the SDIO interface. The ability to force the control of the gated clocks from within the WLAN chip is also provided.

- Function 0 Standard SDIO function (Max BlockSize / ByteCount = 32B)
- Function 1 Backplane Function to access the internal System On Chip (SOC) address space (Max BlockSize / ByteCount = 64B)
- Function 2 WLAN Function for efficient WLAN packet transfer through DMA (MaxBlock Size/ByteCount = 512B)

SDIO Pin Description

SD 4-Bit Mode	
DATA0	Data Line 0
DATA1	Data Line 1 or Interrupt
DATA2	Data Line 2 or Read Wait
DATA3	Data Line 3
CLK	Clock
CMD	Command Line

10. Recommended Reflow Profile



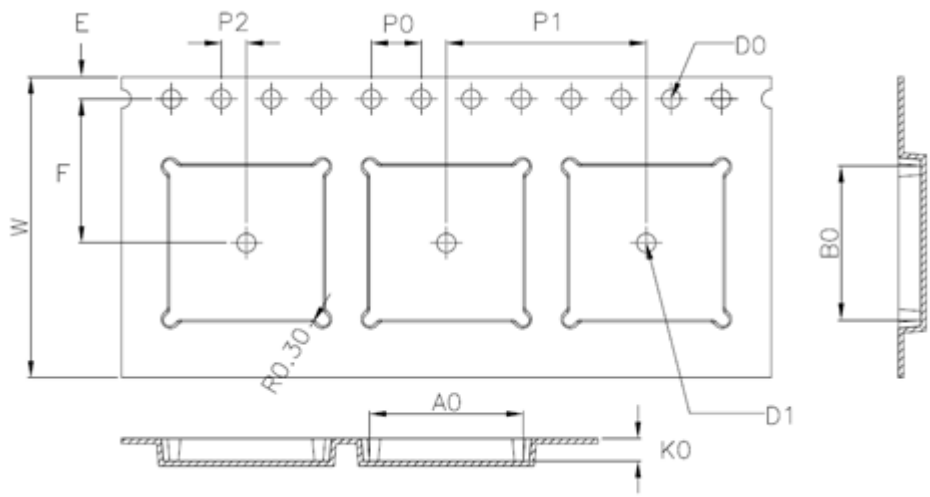
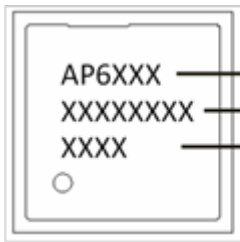
- Referred to IPC/JEDEC standard
- Peak Temperature : <260°C
- Cycle of Reflow: 2 times max.
- The notification of WiFi module before mounting:
The aperture of stencil should be larger than foot print of module, and the stencil thickness should be not less than 0.12mm.
- Adding Nitrogen (N₂) to implement 2000ppm or less of oxygen concentration during reflow process is recommended.
- If the shelf time is exceeded, be sure baking step to remove the moisture from the component.

10.1 Caution for SMT Preparation

Moisture Sensitivity Level: 4

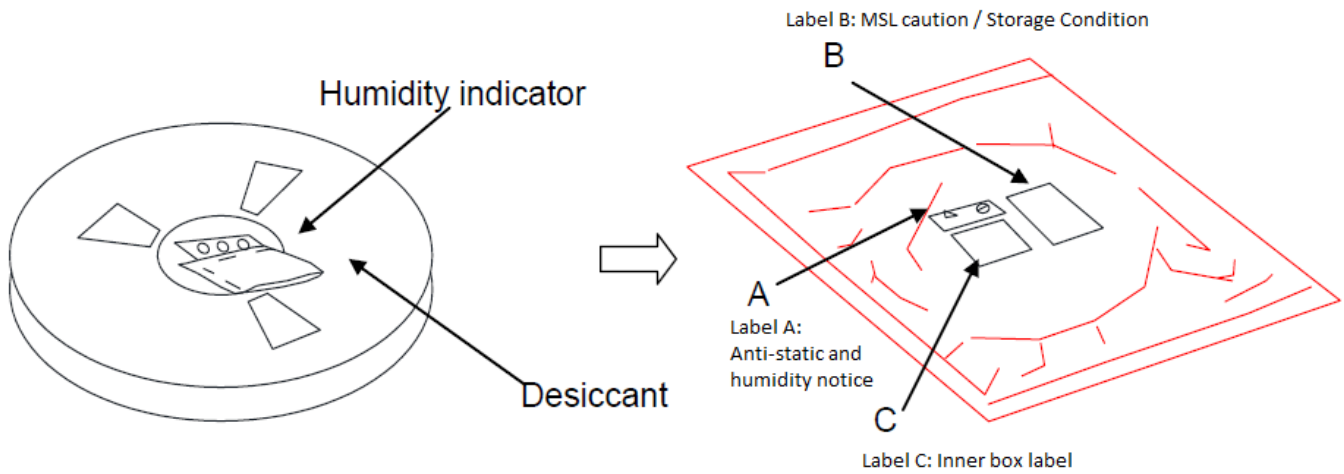
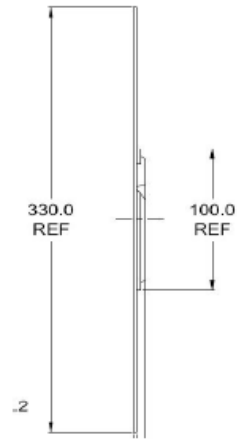
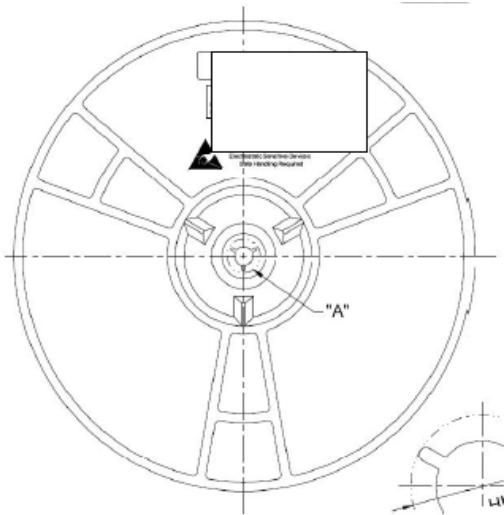
1. Calculated shelf life in sealed bag: 12 months at $<40^{\circ}\text{C}$ and $<90\%$ relative humidity (RH).
2. Peak package body temperature: 250°C .
3. After bag was opened, devices that will be subjected to reflow solder or other high temperature process must be
 - a) Mounted within: 72 hours of factory conditions $\leq 30^{\circ}\text{C}/60\%RH$ or
 - b) Stored per J-STD-033
4. Devices require bake before mounting, if:
 - a) Humidity Indicator Card reads $> 10\%$ for level 2a - 5a devices or $>60\%$ for level 2 devices when read at $23\pm 5^{\circ}\text{C}$
 - b) 3a or 3b are not met.
5. If baking is required, refer to IPC/JEDEC J-STD-033 for bake procedure.
6. If baking is required, devices may be baked for 7 hours at $125\pm 10^{\circ}\text{C}$

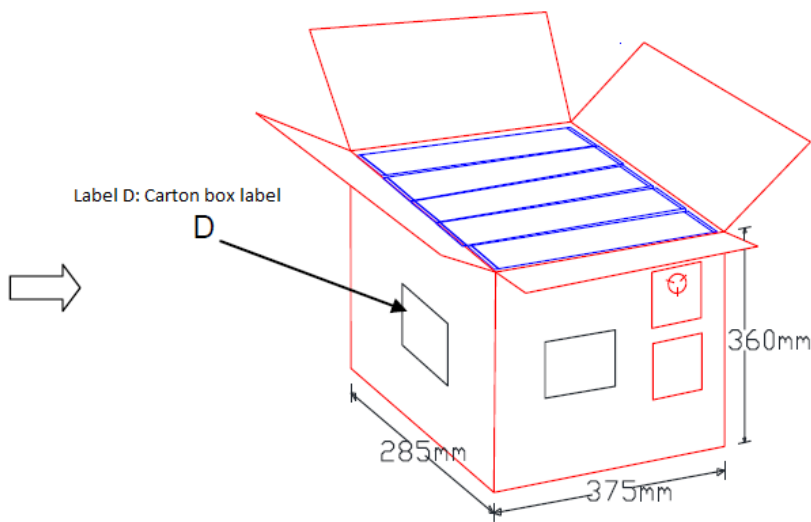
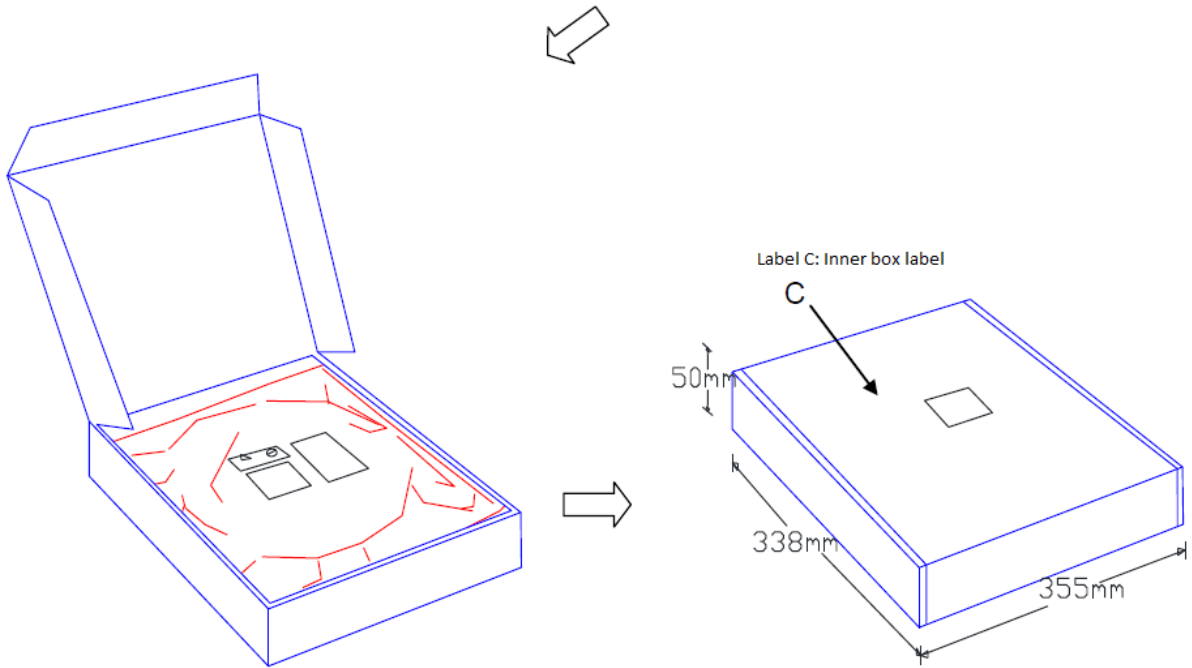
11. Package Information



W	24.00±0.30
A0	12.30±0.10
B0	12.30±0.10
K0	1.80±0.10
E	1.75±0.10
F	11.50±0.10
P0	4.00±0.10
P1	16.00±0.10
P2	2.00±0.10
D0	1.50 $\begin{matrix} +0.10 \\ -0.00 \end{matrix}$
D1	∅1.50MIN

- 10 sprocket hole pitch cumulative tolerance ± 0.20 .
- Carrier camber is within 1 mm in 250 mm.
- Material: Black Conductive Polystyrene Alloy.
- All dimensions meet EIA-481-D requirements.
- Thickness: 0.30 ± 0.05 mm.
- Packing length per 22" reel: 98.5 Meters.(1:3)
- Component load per 13" reel : 1500 PCS





Note: 1 tape reel = 1 box = 1,500pcs
1 Carton = 5 box = 7,500pcs

12. Ordering Information

Product Name	Part Number	Description
AP6212A	R9701920009	11b/g/n 1T1R WiFi + Bluetooth5.2 Combo Sip Module