Datasheet

AP6212SD

IEEE 802.11b/g/n 1x1

WiFi with Bluetooth5.2 M.2 LGA Type 1216 Module

The revision history of the product specification

Version	Purpose	Date	Editor
1.0	Initial Doc	2019/10/16	Aaron
1.1	Correcting document content (Page 4)	2020/03/31	Kamoro
1.2	Correcting document content (Page 4)	2021/04/20	kamoro
1.3	Modify BT Spec & Operating temperature	2023/04/14	Aaron

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Contents

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1. Introduction

1.1 Product Overview

AP6212SD is 11b/g/n 1T1R WiFi +Bluetooth 5.2 WiFi module. It's a highly integrated single-chip solution and provides the highest level of integration for a mobile or handheld wireless system. offers the low-cost in the industry for smartphones, tablets, and a wide range of other portable devices. The WiFi module is designed to address the needs of highly mobile devices that require minimal power consumption and compact size. It implements the world's most advanced Enhanced Collaborative Coexistence algorithms and hardware mechanisms, allowing for an extremely collaborative WLAN and Bluetooth coexistence.

It can achieve up to a speed of 72.2Mbps with single stream in 802.11n draft, 54Mbps as specified in IEEE 802.11g, or 11Mbps for IEEE 802.11b to connect to the wireless LAN. The integrated module provides SDIO interface for WiFi, UART / I2S / PCM interface for Bluetooth.

This compact module is a total solution for a combination of WiFi + BT technologies. The module is specifically developed for Smart phones and Portable devices.

1.2 Product Feature

1.2.1 WLAN

- Single-band 2.4GHz IEEE 802.11b/g/n
- Supports standard interfaces SDIO v2.0(50MHz, 4-bit and 1-bit)
- Simultaneous BT/WLAN receive with single antenna
- Concurrent Bluetooth and WLAN operation
- IEEE Co-existence technologies are integrated die solution

1.2.2 Bluetooth

- BT host digital interface:
  - UART (up to 4 Mbps)
  - PCM for audio data
- ECI - enhanced coexistence support, ability to coordinate BT SCO transmissions around WLAN receives

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2.Specification

2.1 General Specification

Standards	IEEE 802.11b/g/n WiFi+BT5.2 Module Bluetooth V5.2, V4.1, V4.0 LE, V3.0+HS, V2.1+EDR
Chipset	Synaptics
Operating Frequency	2.400 GHz ~ 2.4835 GHz (2.4GHz ISM Band) Bluetooth: 2.402 GHz ~ 2.480 GHz
Modulation	WiFi: 802.11b: DSSS (DBPSK, DQPSK, CCK) 802.11g: OFDM (BPSK, QPSK, 16-QAM, 64-QAM) 802.11gn: OFDM (BPSK, QPSK, 16-QAM, 64-QAM) BT: Header: GFSK Payload 2M: π/4-DQPSK Payload 3M: 8-DPSK
Interface	WLAN: SDIO 2.0 Bluetooth: UART / PCM
Form Factor	Stamp Type
Antenna	1 x IPEX MHF4 connector
Dimension	L x W x H: 12mm(± 0.15mm) x 16mm(± 0.15mm) x 1.52mm(typical)
Operating temperature	-40°C~85°C
Storage temperature	-40°C~85°C
Humidity (Non-Condensing)	10%~95% (Operating)
Weight	0.56g
Driver Support	Linux, Android

Note: The optimal RF performance specified in the data sheet, however, is guaranteed only for -10℃ to 55℃.

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2.2 WiFi 2.4GHz RF Specification

Conditions: VBAT=3.3V; VDDIO=3.3V; Temp:25℃

Output Power	802.11b /11Mbps : 16 dBm ± 1.5 dB @ EVM ≤ -9dB	
	802.11g /54Mbps : 15 dBm ± 1.5 dB @ EVM ≤ -25dB	
	802.11n /65Mbps : 14 dBm ± 1.5 dB @ EVM ≤ -27dB	
Receive Sensitivity (11n,20MHz) @10% PER	- MCS=0	PER @ -85 dBm, ± 2 dB
	- MCS=1	PER @ -84 dBm, ± 2 dB
	- MCS=2	PER @ -82 dBm, ± 2 dB
	- MCS=3	PER @ -80 dBm, ± 2 dB
	- MCS=4	PER @ -77 dBm, ± 2 dB
	- MCS=5	PER @ -73 dBm, ± 2 dB
	- MCS=6	PER @ -71 dBm, ± 2 dB
	- MCS=7	PER @ -68 dBm, ± 2 dB
Receive Sensitivity (11g) @10% PER	- 6Mbps	PER @ -86 dBm, ± 2 dB
	- 9Mbps	PER @ -85 dBm, ± 2 dB
	- 12Mbps	PER @ -85 dBm, ± 2 dB
	- 18Mbps	PER @ -83 dBm, ± 2 dB
	- 24Mbps	PER @ -81 dBm, ± 2 dB
	- 36Mbps	PER @ -78 dBm, ± 2 dB
	- 48Mbps	PER @ -73 dBm, ± 2 dB
	- 54Mbps	PER @ -71 dBm, ± 2 dB
Receive Sensitivity (11b) @8% PER	- 1Mbps	PER @ -90 dBm, ± 2 dB
	- 2Mbps	PER @ -88 dBm, ± 2 dB
	- 5.5Mbps	PER @ -87 dBm, ± 2 dB
	- 11Mbps	PER @ -84 dBm, ± 2 dB
Data Rate	802.11b : 1, 2, 5.5, 11Mbps	
	802.11g : 6, 9, 12, 18, 24, 36, 48, 54Mbps	
Data Rate (20MHz ,Long GI,800ns)	802.11n: 6.5, 13, 19.5, 26, 39, 52, 58.5, 65Mbps	
Data Rate (20MHz ,short GI,400ns)	802.11n : 7.2, 14.4, 21.7, 28.9, 43.3, 57.8, 65,72.2Mbps	
Maximum Input Level	802.11b : -10 dBm	
	802.11g/n : -20 dBm	
Antenna Reference	Small antennas with 0~2 dBi peak gain	

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2.3 Bluetooth RF Specification

Conditions: VBAT=3.3V ; VDDIO=3.3V ; Temp:25℃

RF Specification			
	Min	**Typical**	**Max**
Output Power*		7	
Sensitivity @ BER=0.1% for GFSK (1Mbps)		-86 dBm	
Sensitivity @ BER=0.01% for π/4-DQPSK (2Mbps)		-86 dBm	
Sensitivity @ BER=0.01% for 8DPSK (3Mbps)		-80 dBm	
Maximum Input Level	GFSK (1Mbps):-20dBm		
	π/4-DQPSK (2Mbps) :-20dBm		
	8DPSK (3Mbps) :-20dBm		

Note*：The Bluetooth output power is able to be configured by firmware (hcd file).

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3. Electrical Characteristics

3.1 Absolute Maximum Ratings

Symbol	Description	Min.	Max.	Unit
VBAT	Input supply Voltage	-0.5	5.5	V
VDDIO	Digital/Bluetooth/SDIO/ I/O Voltage	-0.5	3.6	V

3.2 Recommended Operating Rating

The module requires two power supplies: VBAT and VDDIO.

Voltage rails	Min.	Typ.	Max.	Unit
Operating Temperature	-10	25	65	deg.C
VBAT	3.0	3.3	3.8	V
VDDIO	1.7	3.3	3.6	V

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3.3 Recommended Operating Conditions and DC Characteristics

Parameter	Symbol	Value			Unit
		Minimum	Typical	Maximum	
DC supply voltage for VBAT	VBAT	3.0[a]	-	4.8[b]	V
DC supply voltage for core	VDD	1.14	1.2	1.26	V
DC supply voltage for RF blocks in chip	VDDRF	1.14	1.2	1.26	V
DC supply voltage for digital I/O	VDDIO VDDIO_SD	1.71	-	3.63	V
DC supply voltage for RF switch I/Os	VDDIO_RF	3.13	3.3	3.46	V
External TSSI input	TSSI	0.15	-	0.95	V
Internal POR threshold	Vth_POR	0.4	-	0.7	V
Other Digital I/O Pins					
For VDDIO = 1.8V					
Input high voltage	VIH	1.27	--	-	V
Input low voltage	VIL	-	-	0.58	V
Output high Voltage @ 2 mA	VOH	1.40	-	-	V
Output Low Voltage @ 2 mA	VOL	-	-	0.45	V
For VDDIO = 3.3V					
Input high voltage	VIH	0.625 x VDDIO	-	-	V
Input low voltage	VIL	-	-	0.25 x VDDIO	V
Output high Voltage @ 2 mA	VOH	0.75 x VDDIO	-	-	V
Output Low Voltage @ 2 mA	VOL	-	-	0.125 x VDDIO	V
Other Digital I/O Pins					
For VDDIO=1.8V					
Input high voltage	VIH	0.65 x VDDIO	-	-	V
Input low voltage	VIL	-	-	0.35 x VDDIO	V
Output high voltage @2mA	VOH	VDDIO-0.45	-	-	V
Output low voltage @2mA	VOL	-	-	0.45	V
For VDDIO=3.3V		-	-	-	
Input high voltage	VIH	2.00	-	-	V
Input low voltage	VIL	-	-	0.80	V
Output high voltage@2mA	VOH	VDDIO-0.4	-	-	V
Output low voltage@2mA	VOL	-	-	0.4	V

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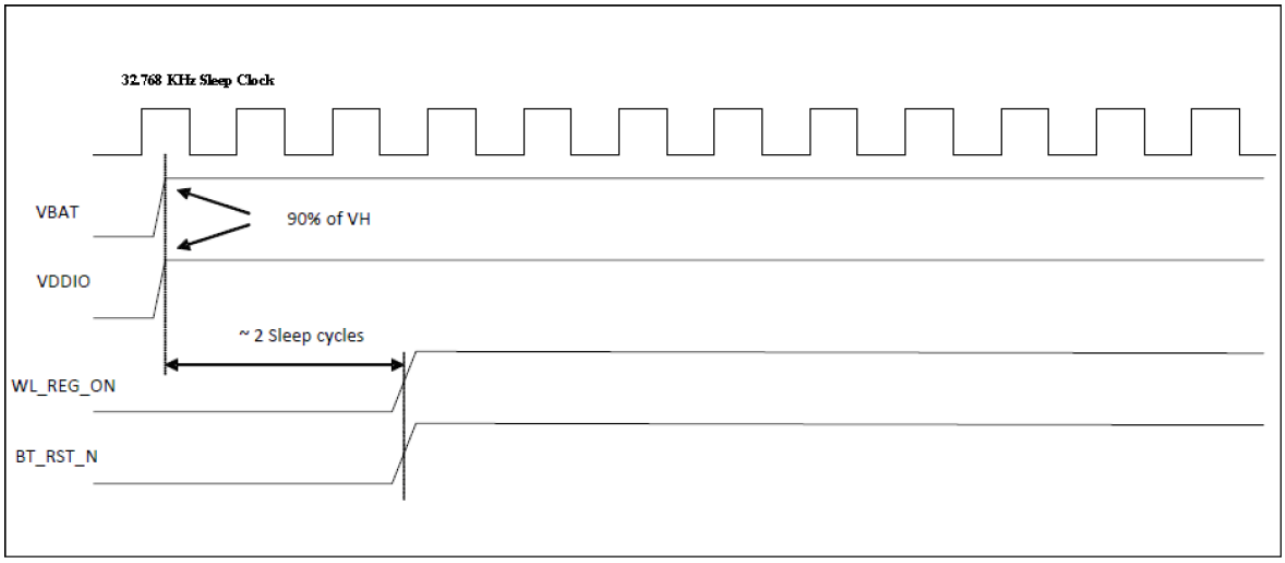
4. Host Interface Timing Diagram

4.1 Power-up Sequence Timing Diagram

The module has signals that allow the host to control power consumption by enabling or disabling the Bluetooth, WLAN and internal regulator blocks. These signals are described below. Additionally, diagrams are provided to indicate proper sequencing of the signals for carious operating states. The timing value indicated are minimum required values: longer delays are also acceptable.

- WL_REG_ON: Used by the PMU to power up the WLAN section. When this pin is high, the regulators are enabled and the WLANsection is out of reset. When this pin is low the WLAN section is in reset.
- BT_RST_N: Low asserting reset for Bluetooth. This pin has no effect on WLAN and does not control any PMU functions. This pin must be driven high or low (not left floating).



WLAN=ON, Bluetooth=ON

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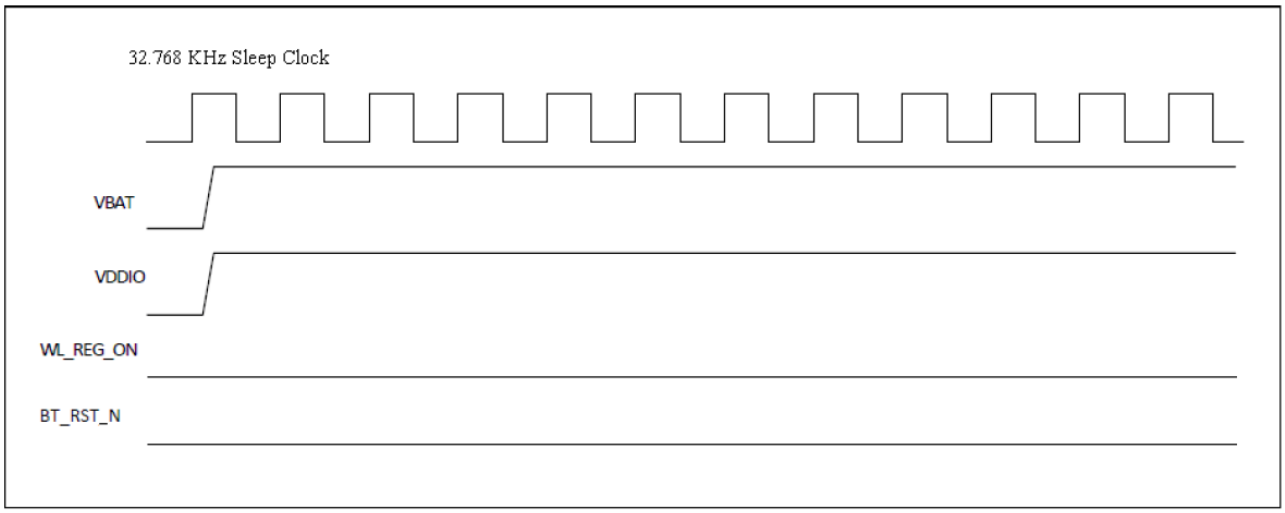
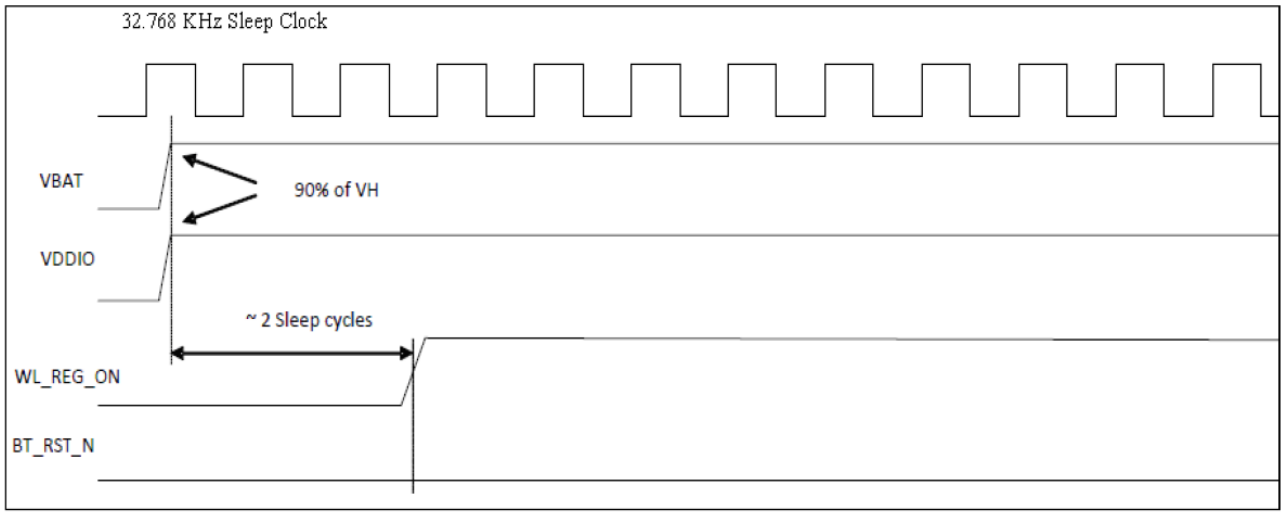


WLAN=OFF, Bluetooth=OFF



WLAN=ON, Bluetooth=OFF

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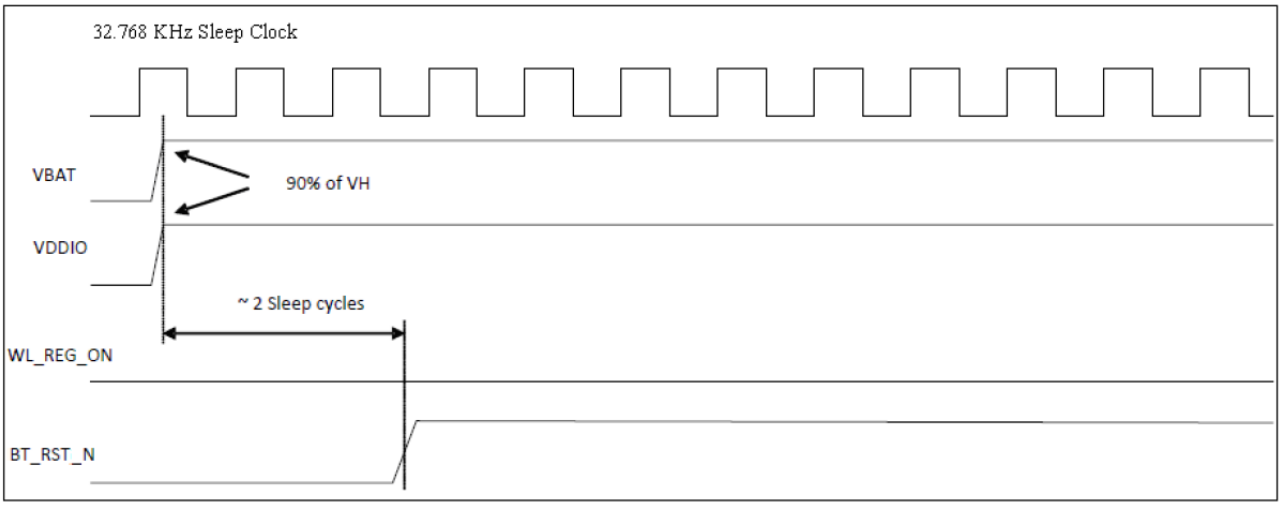
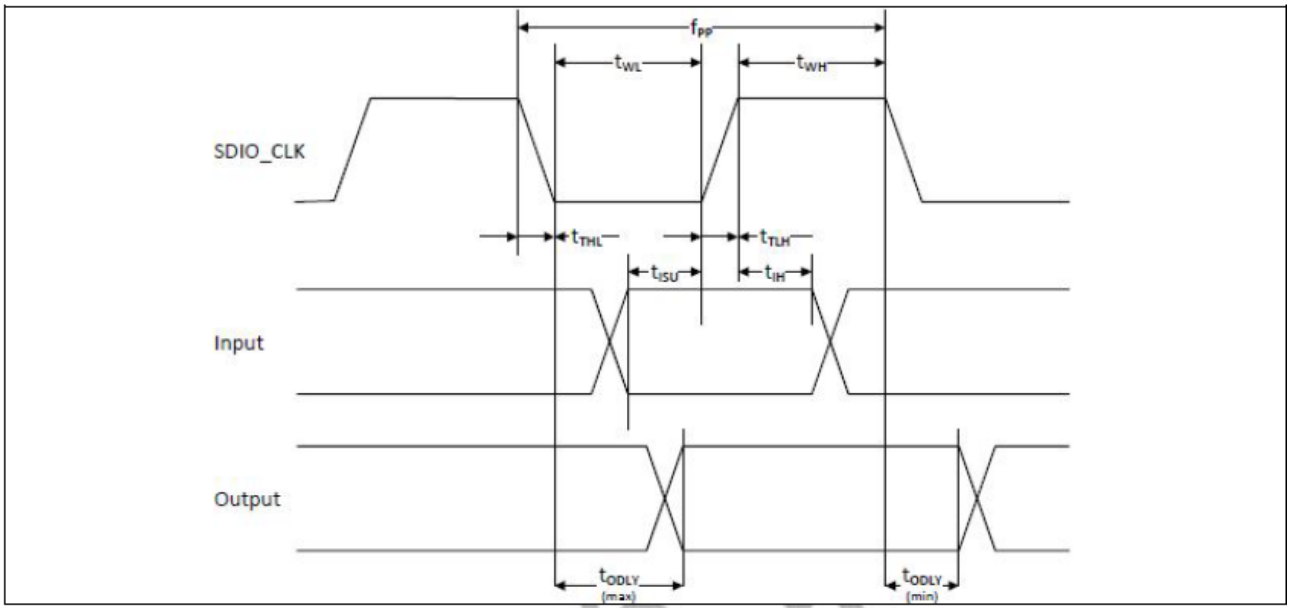


WLAN=OFF, Bluetooth=ON

4.2 SDIO Default Mode Timing Diagram



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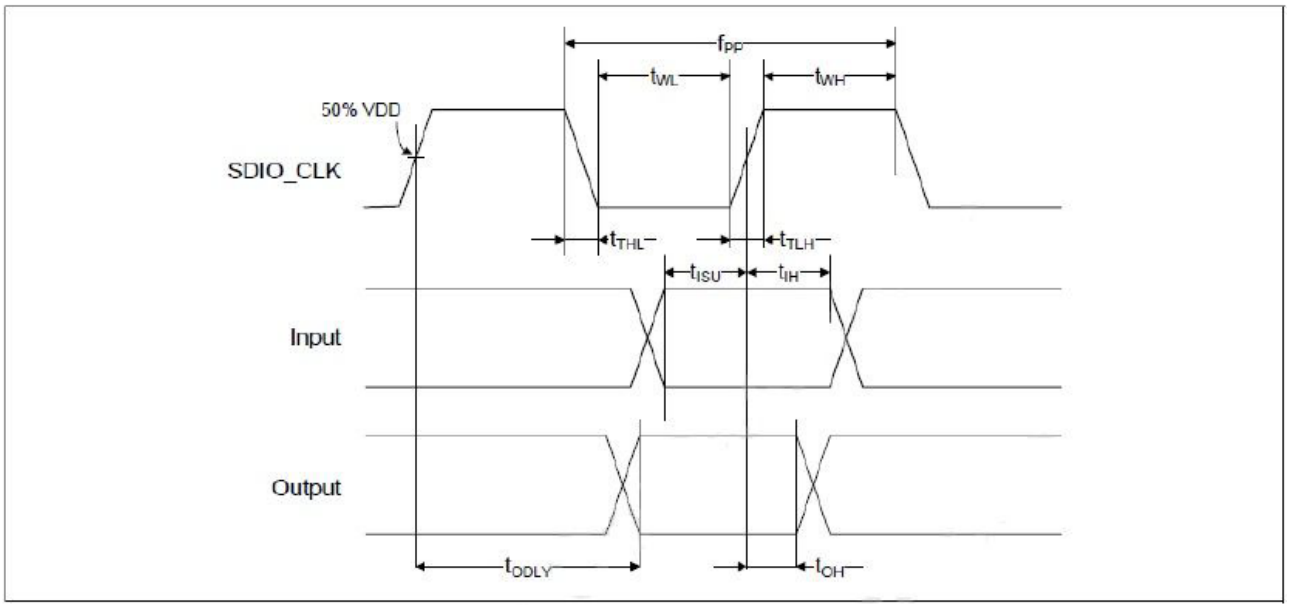
Parameter	Symbol	Minimum	Typical	Maximum	Unit
SDIO CLK (ALL values are referred to minimum VIH and maximum VIL[b])					
Frequency – Data Transfer mode	fPP	0	-	25	MHz
Frequency – Identification mode	fOD	0	-	400	kHz
Clock low time	tWL	10	-	-	ns
Clock high time	tWH	10	-	-	ns
Clock rise time	tTLH	-	-	10	ns
Clock low time	tTHL	-	-	10	ns
Inputs：CMD, DAT(referenced to CLK)					
Input setup time	tISU	5	-	-	ns
Input hold time	tIH	5	-	-	ns
Outputs：CMD, DAT(referenced to CLK)					
Output delay time - Data Transfer mode	tODLY	0	-	14	ns
Output delay time,- Identification mode	tODLY	0	-	50	ns

a. Timing is based on CL ≤ 40 pF load on CMD and Data.

b. Min. (Vih) = 0.7 x VDDIO and max. (Vil) = 0.2 x VDDIO

4.3 SDIO High Speed Mode Timing Diagram



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Parameter	Symbol	Minimum	Typical	Maximum	Unit
SDIO CLK (ALL values are referred to minimum VIH and maximum VIL[b])					
Frequency – Data Transfer mode	fPP	0	-	50	MHz
Frequency – Identification mode	fOD	0	-	400	kHz
Clock low time	tWL	7	-	-	ns
Clock high time	tWH	7	-	-	ns
Clock rise time	tTLH	-	-	3	ns
Clock low time	tTHL	-	-	3	ns
Inputs：CMD, DAT(referenced to CLK)					
Input setup time	tISU	6	-	-	ns
Input hold time	tIH	2	-	-	ns
Outputs：CMD, DAT(referenced to CLK)					
Output delay time - Data Transfer mode	tODLY	-	-	14	ns
Output hold time	tOH	2.5	-	-	ns
Total system capacitance(each line)	CL			40	pF

a. Timing is based on CL <= 40pF load on CMD and Data.
b. Min(Vih) = 0.7 x VDDIO and max(Vil) = 0.2 x VDDIO

4.4 PCM Interface Description

The PCM Interface on the BCM4343 can connect to linear PCM Codec devices in master or slave mode. In master mode, the BCM4343 generates the PCM_CLK and PCM_SYNC signals, and in slave mode, these signals are provided by another master on the PCM interface and are inputs to the BCM4343.The configuration of the PCM interface may be adjusted by the host through the use of vendor-specific HCI commands

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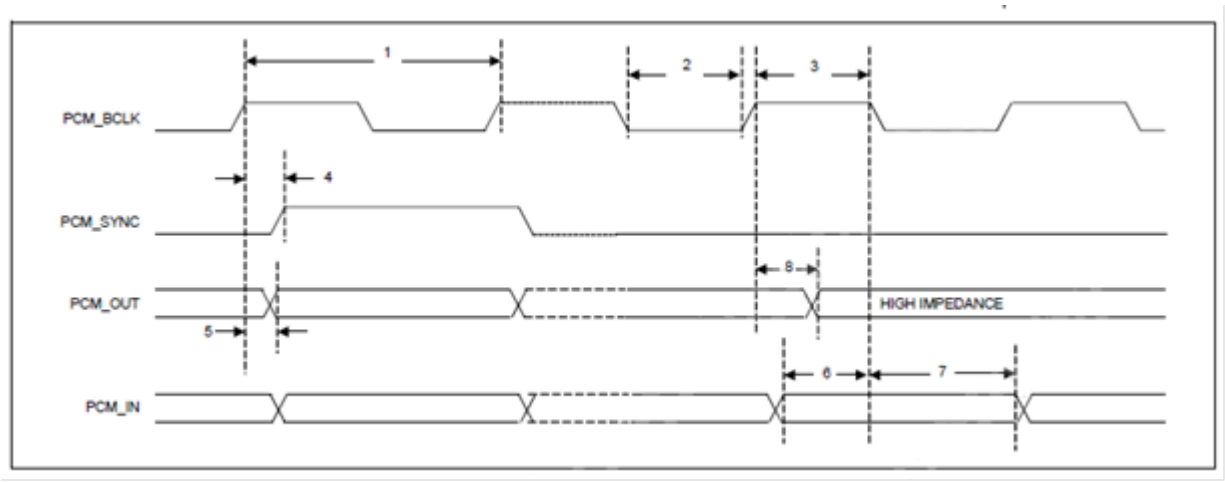
Short Frame Sync, Master Modem

PCM Timing Diagram (Short Frame Sync, Master Mode)



PCM Interface Timing Specifications (Short Frame Sync, Master Mode)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency		-	12	MHz
2	PCM bit clock low	41	-	-	ns
3	PCM bit clock high	41	-	-	ns
4	PCM_SYNC delay	0	-	25	ns
5	PCM_OUT delay	0	-	25	ns
6	PCM_IN setup	8	-	-	ns
7	PCM_IN hold	8	-	-	ns
8	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	-	25	ns

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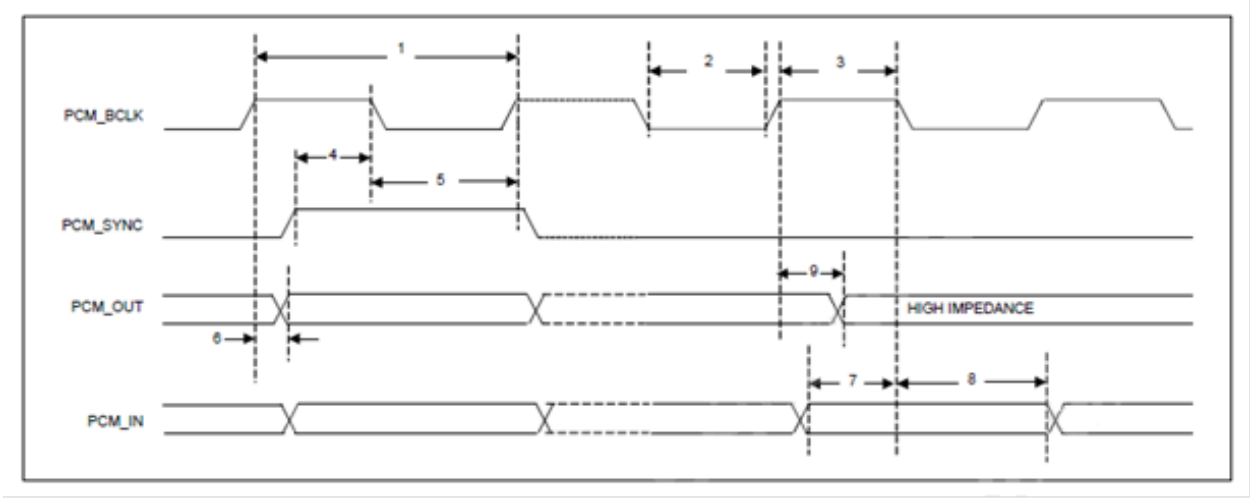
Short Frame Sync, Slave Mode

PCM Timing Diagram (Short Frame Sync, Slave Mode)



PCM Interface Timing Specifications (Short Frame Sync, Slave Mode)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency		-	12	MHz
2	PCM bit clock low	41	-	-	ns
3	PCM bit clock high	41	-	-	ns
4	PCM_SYNC setup	8	-	-	ns
5	PCM_SYNC hold	8	-	-	ns
6	PCM_OUT delay	0	-	25	ns
7	PCM_IN setup	8	-	-	ns
8	PCM_IN hold	8	-	-	ns
9	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	-	25	ns

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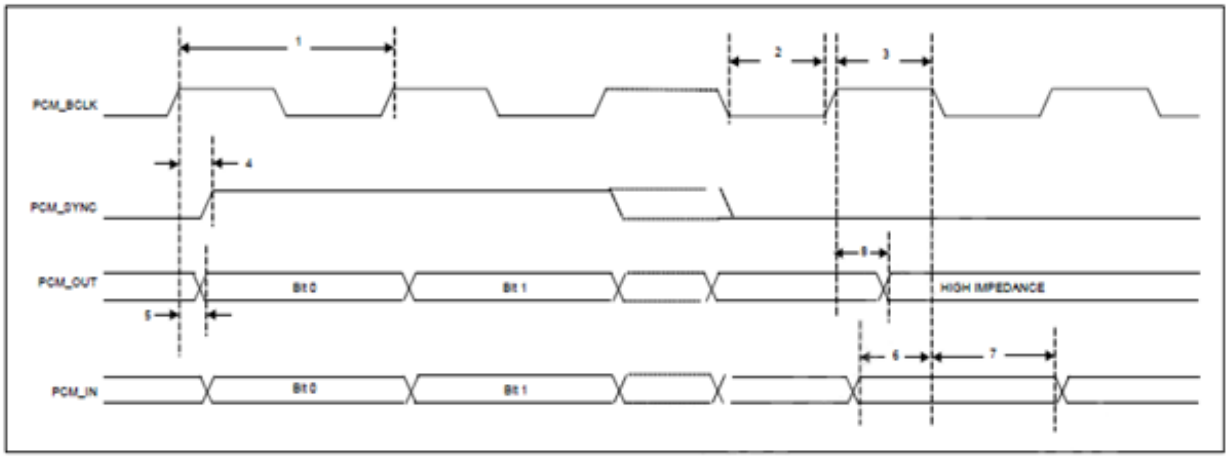
Long Frame Sync, Master Mode

PCM Timing Diagram (Long Frame Sync, Master Mode)



PCM Interface Timing Specifications (Long Frame Sync, Master Mode)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency		-	12	MHz
2	PCM bit clock low	41	-	-	ns
3	PCM bit clock high	41	-	-	ns
4	PCM_SYNC delay	0	-	25	ns
5	PCM_OUT delay	0	-	25	ns
6	PCM_IN setup	8	-	-	ns
7	PCM_IN hold	8	-	-	ns
8	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	-	25	ns

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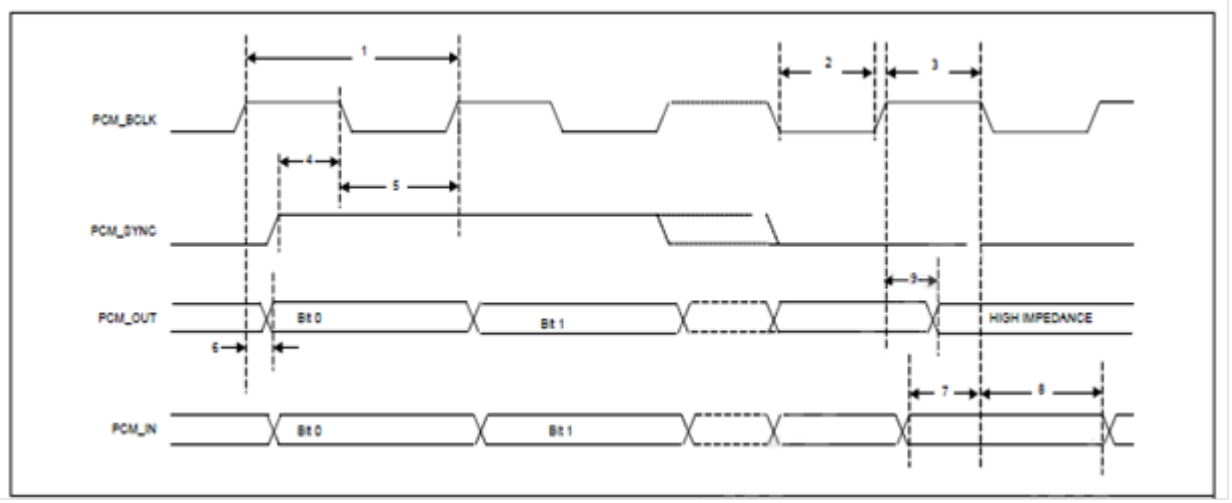
Long Frame Sync, Slave Mode

PCM Timing Diagram (Long Frame Sync, Slave Mode)



PCM Interface Timing Specifications (Long Frame Sync, Slave Mode)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency		-	12	MHz
2	PCM bit clock low	41	-	-	ns
3	PCM bit clock high	41	-	-	ns
4	PCM_SYNC setup	8	-	-	ns
5	PCM_SYNC hold	8	-	-	ns
6	PCM_OUT delay	0	-	25	ns
7	PCM_IN setup	8	-	-	ns
8	PCM_IN hold	8	-	-	ns
9	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	-	25	ns

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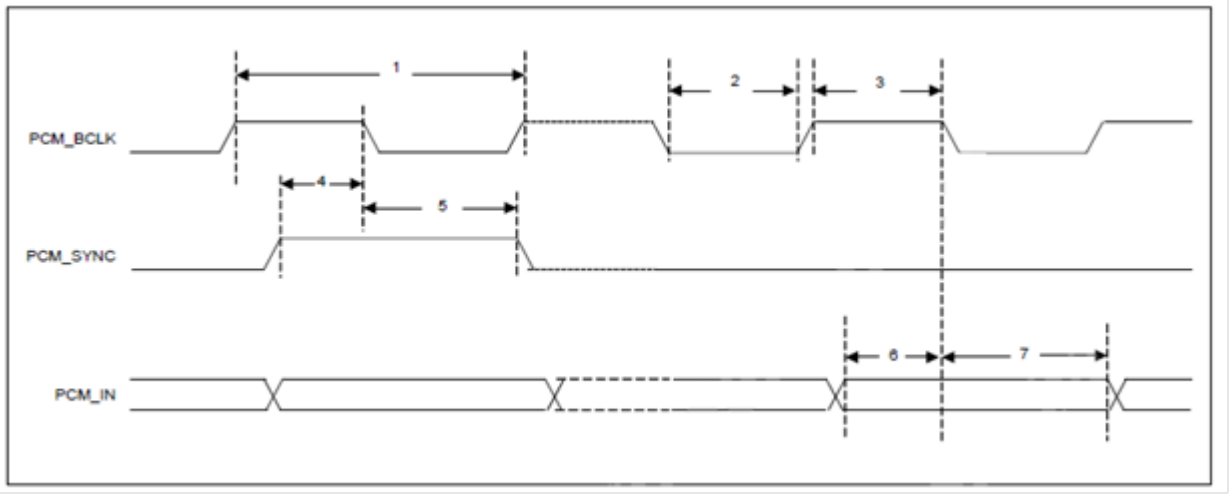
Short Frame Sync, Burst Mode

PCM Burst Mode Timing (Receive Only, Short Frame Sync)

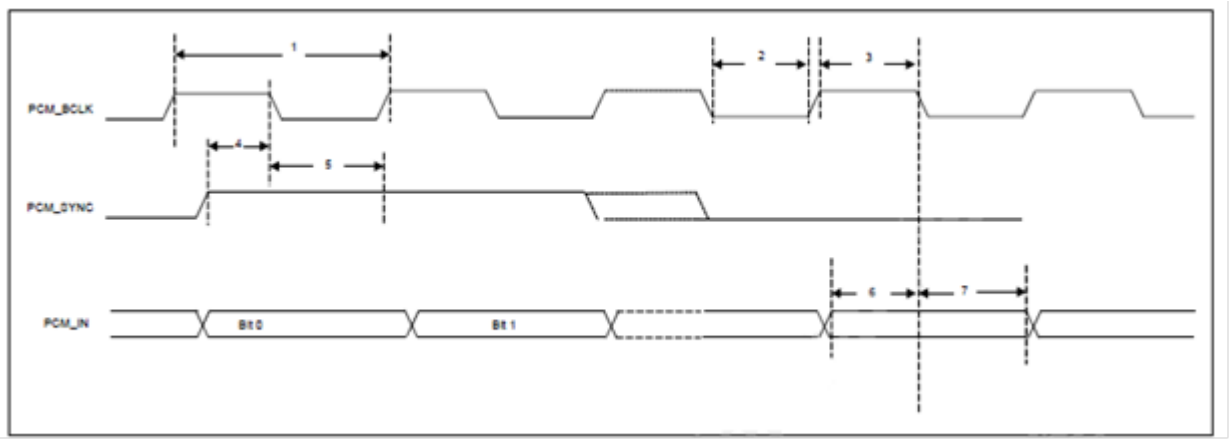


PCM Burst Mode (Receive Only, Short Frame Sync)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency		-	24	MHz
2	PCM bit clock low	20.8	-	-	ns
3	PCM bit clock high	20.8	-	-	ns
4	PCM_SYNC setup	8	-	-	ns
5	PCM_SYNC hold	8	-	-	ns
6	PCM_IN setup	8	-	-	ns
7	PCM_IN hold	8	-	-	ns

Long Frame Sync, Burst Mode

PCM Burst Mode Timing (Receive Only, Long Frame Sync)



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PCM Burst Mode (Receive Only, Long Frame Sync)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency		-	24	MHz
2	PCM bit clock low	20.8	-	-	ns
3	PCM bit clock high	20.8	-	-	ns
4	PCM_SYNC setup	8	-	-	ns
5	PCM_SYNC hold	8	-	-	ns
6	PCM_IN setup	8	-	-	ns
7	PCM_IN hold	8	-	-	ns

4.5 UART Interface Description

The UART is a standard 4-wire interface (RX, TX, RTS, and CTS) with adjustable baud rates from 9600 bps to 4.0 Mbps. The interface features an automatic baud rate detection capability that returns a baud rate selection. Alternatively, the baud rate may be selected through a vendor-specific UART HCI command.

UART has a 1040-byte receive FIFO and a 1040-byte transmit FIFO to support EDR. Access to the FIFOs is conducted through the AHB interface through either DMA or the CPU. The UART supports the Bluetooth 5.0 UART HCI specification: H4, a custom Extended H4, and H5. The default baud rate is 115.2 Kbaud.

The UART supports the 3-wire H5 UART transport, as described in the Bluetooth specification (Three-wire UART Transport Layer). Compared to H4, the H5 UART transport reduces the number of signal lines required by eliminating the CTS and RTS signals.

The BCM4343 UART can perform XON/XOFF flow control and includes hardware support for the Serial Line Input Protocol (SLIP). It can also perform wake-on activity. For example, activity on the RX or CTS inputs can wake the chip from a sleep state.

Normally, the UART baud rate is set by a configuration record downloaded after device reset, or by automatic baud rate detection, and the host does not need to adjust the baud rate. Support for changing the baud rate during normal HCI UART operation is included through a vendor-specific command that allows the host to adjust the contents of the baud rate registers. The BCM4343 UARTs operate correctly with the host UART as long as the combined baud rate error of the two devices is within ±2%.

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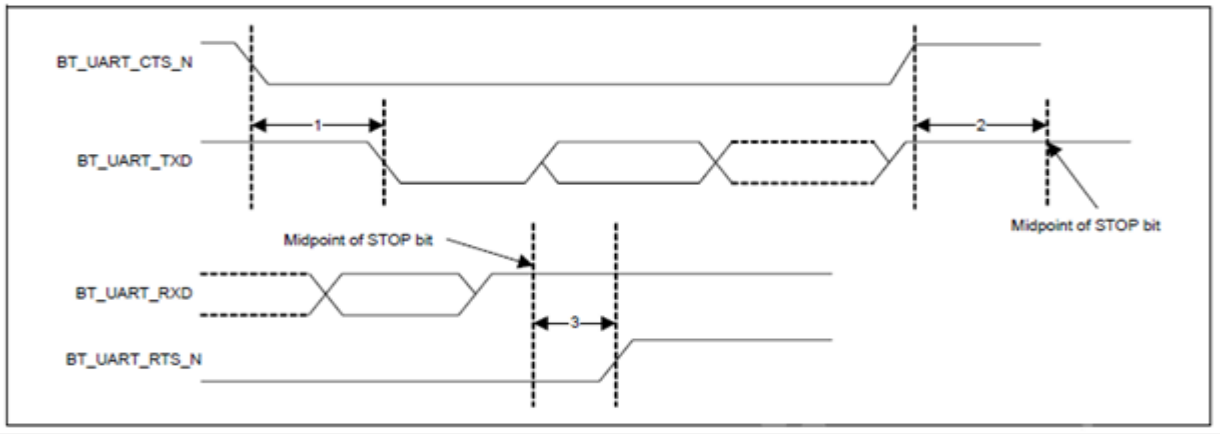
Example of Common Baud Rates

Desired Rate	Actual Rate	Error(%)
4000000	4000000	0.00
3692000	3692308	0.01
3000000	3000000	0.00
2000000	2000000	0.00
1500000	1500000	0.00
1444444	1454544	0.70
921600	923077	0.16
460800	461538	0.16
230400	230796	0.17
115200	115385	0.16
57600	57692	0.16
38400	38400	0.00
28800	28846	0.16
19200	19200	0.00
14400	14423	0.16
9600	9600	0.00

UART Timing



UART Timing Specifications

Pef	Characteristics	Min.	Typ.	Max.	Unit
1	Delay time, BT_UART_CTS_N low BT_UART_TXD valid	-	-	1.5	Bit periods
2	Setup time, BT_UART_CTS_N high before midpoint stop bit	-	-	0.5	Bit periods
3	Delay time, midpoint of stop bit BT_UART_RTS_N high	-	-	0.5	Bit periods

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5. Power Consumption

■ **2.4GHz:**

Test Mode	DUT Status	Supply Voltage	Test Data
802.11b mode	Continue TX	VBAT	310
	Continue RX	VBAT	41
802.11g mode	Continue TX	VBAT	230
	Continue RX	VBAT	40
802.11n mode	Continue TX	VBAT	212
	Continue RX	VBAT	39
Bluetooth mode	Continue TX	VBAT	6.7
	Continue RX	VBAT	6.7

(Unit: mA)

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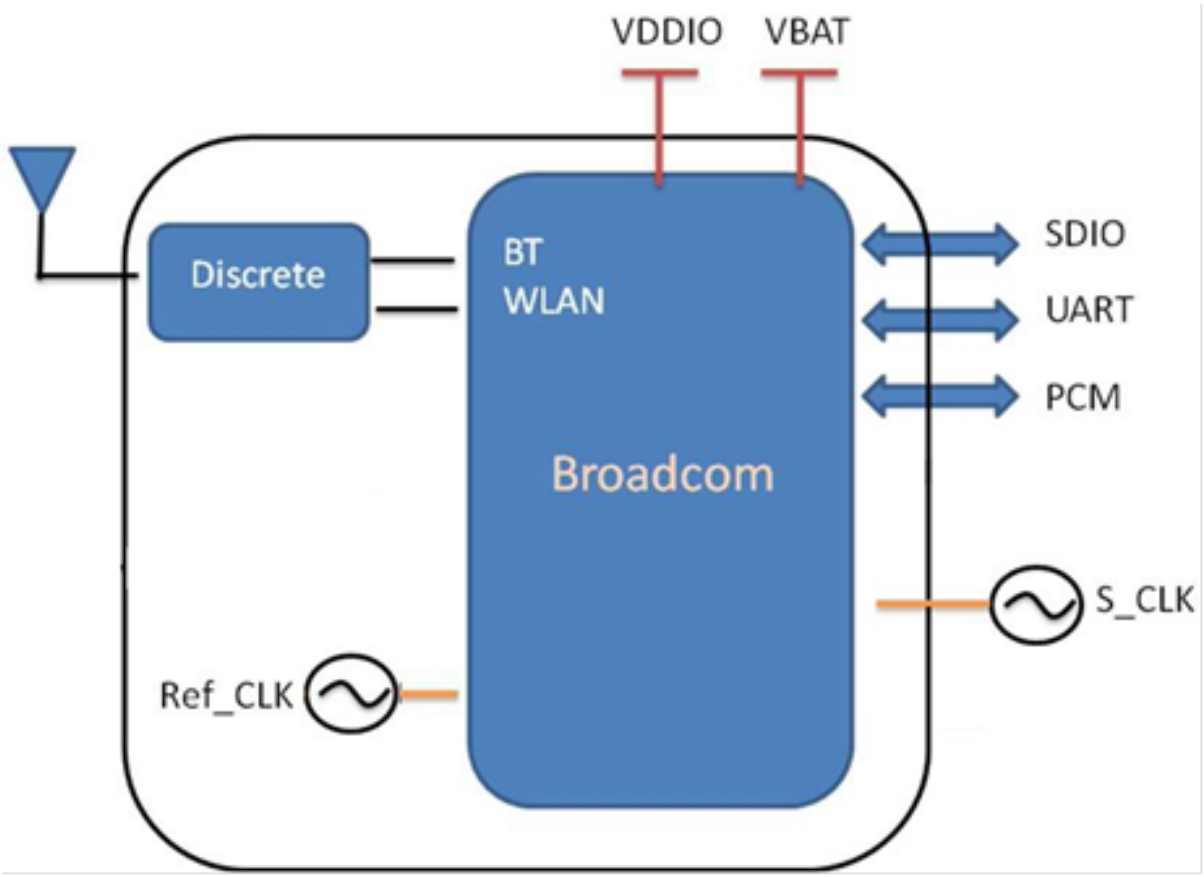
6. Block Diagram



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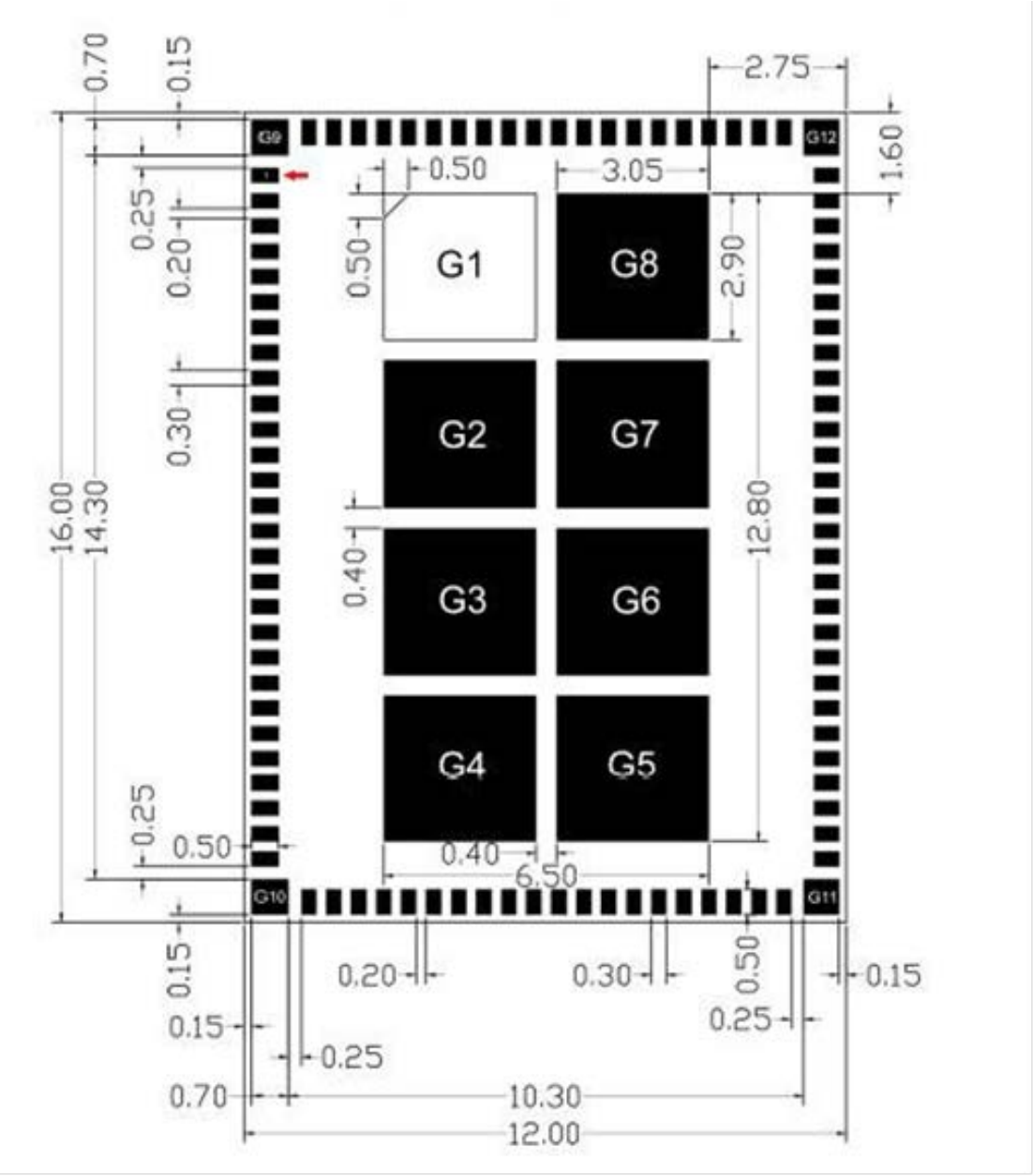
7. Pin Definition

7.1 Pin Map

<TOP VIEW >



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7.2 Pin Definition

NO	Name	Type	Description
1	NC	—	Floating(Don't connect to ground)
2	NC	—	Floating(Don't connect to ground)
3	NC	—	Floating(Don't connect to ground)
4	NC	—	Floating(Don't connect to ground)
5	VBAT	I	VBAT system power supply input
6	GND	—	Ground connections
7	NC	—	Floating(Don't connect to ground)
8	NC	—	Floating(Don't connect to ground)
9	NC	—	Floating(Don't connect to ground)
10	NC	—	Floating(Don't connect to ground)
11	GPIO1	I/O	FOR LTE COEX GPIO, (if no used, just floating)
12	NC	—	Floating(Don't connect to ground)
13	GPIO2	I/O	FOR LTE COEX GPIO, (if no used, just floating)
14	NC	—	Floating(Don't connect to ground)
15	NC	—	Floating(Don't connect to ground)
16	NC	—	Floating(Don't connect to ground)
17	GND	—	Ground connections
18	NC	—	Floating(Don't connect to ground)
19	NC	—	Floating(Don't connect to ground)
20	GND	—	Ground connections
21	NC	—	Floating(Don't connect to ground)
22	NC	—	Floating(Don't connect to ground)
23	GND	—	Ground connections
24	BT_DEV_WAKE	I/O	Bluetooth DEV_WAKE
25	NC	—	Floating(Don't connect to ground)
26	GND	—	Ground connections
27	SLP_CLK	I	External sleep clock input (32.768KHz)
28	NC	—	Floating(Don't connect to ground)
29	NC	—	Floating(Don't connect to ground)
30	NC	—	Floating(Don't connect to ground)

31	NC	—	Floating(Don't connect to ground)
32	GND	—	Ground connections
33	NC	—	Floating(Don't connect to ground)
34	NC	—	Floating(Don't connect to ground)
35	GND	—	Ground connections
36	NC	—	Floating(Don't connect to ground)
37	NC	—	Floating(Don't connect to ground)
38	GND	—	Ground connections
39	NC	—	Floating(Don't connect to ground)
40	NC	—	Floating(Don't connect to ground)
41	GND	—	Ground connections
42	NC	—	Floating(Don't connect to ground)
43	BT_I2S_WS	I/O	I2S data command line
44	NC	—	Floating(Don't connect to ground)
45	WL_REG_ON	I	Used by PMU to power up or power down the internal module regulators used by the WLAN section.
46	SDIO_WAKE_L_GPIO_0	I	WL_HOST_WAKE
47	SDIO_DATA3	I/O	SDIO data line bit3
48	SDIO_DATA2	I/O	SDIO data line bit2
49	SDIO_DATA1	I/O	SDIO data line bit1
50	SDIO_DATA0	I/O	SDIO data line bit0
51	SDIO_CMD	I/O	SDIO command/response
52	SDIO_CLK	I	SDIO clock input
53	BT_HOST_WAKE	O	Bluetooth HOST_WAKE
54	UART_CTS	I	UART_CTS
55	UART_SOUT	O	UART_SOUT
56	UART_SIN	I	UART_SIN
57	UART_RTS	O	UART_RTS
58	PCM_SYNC	I/O	PCM sync
59	PCM_IN	I	PCM data in
60	PCM_OUT	O	PCM data out

61	PCM_CLK	I/O	PCM bus clock
62	GND	—	Ground connections
63	BT_ENABLE	I	Used by PMU to power up or power down the internal module regulators used by the Bluetooth section.
64	BT_I2S_DO	O	I2S data line output
65	NC	—	Floating(Don't connect to ground)
66	BT_I2S_DI	I	I2S data line input
67	BT_I2S_CLK	I/O	I2S data line clock
68	GND	—	Ground connections
69	NC	—	Floating(Don't connect to ground)
70	NC	—	Floating(Don't connect to ground)
71	GND	—	Ground connections
72	NC	—	Floating(Don't connect to ground)
73	VIO	I	Digital I/O power supply
74	GND	—	Ground connections
75	GND	—	Ground connections
76	GND	—	Ground connections
77	GND	—	Ground connections
78	GND	—	Ground connections
79	GND	—	Ground connections
80	GND	—	Ground connections
81	GND	—	Ground connections
82	GND	—	Ground connections
83	GND	—	Ground connections
84	NC	—	Floating(Don't connect to ground)
85	GND	—	Ground connections
86	GND	—	Ground connections
87	GND	—	Ground connections
88	GND	—	Ground connections
89	NC	—	Floating(Don't connect to ground)
90	NC	—	Floating(Don't connect to ground)

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91	GND	—	Ground connections
92	GND	—	Ground connections
93	GND	—	Ground connections
94	GND	—	Ground connections
95	GND	—	Ground connections
96	GND	—	Ground connections
G1	GND	—	Ground connections
G2	GND	—	Ground connections
G3	GND	—	Ground connections
G4	GND	—	Ground connections
G5	GND	—	Ground connections
G6	GND	—	Ground connections
G7	GND	—	Ground connections
G8	GND	—	Ground connections

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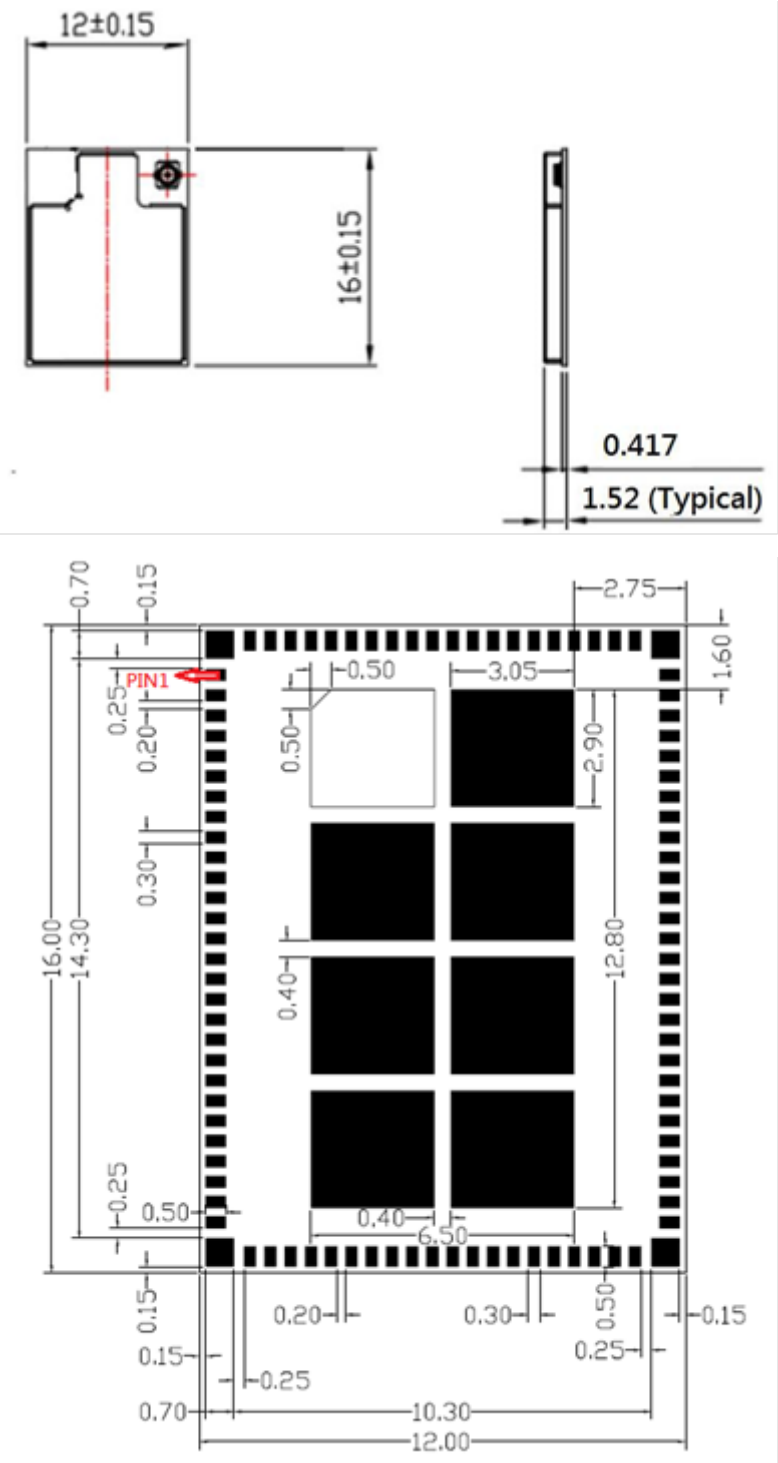
8. Mechanical Specification

8.1 Module Dimension

< TOP VIEW >



(Unit: mm)

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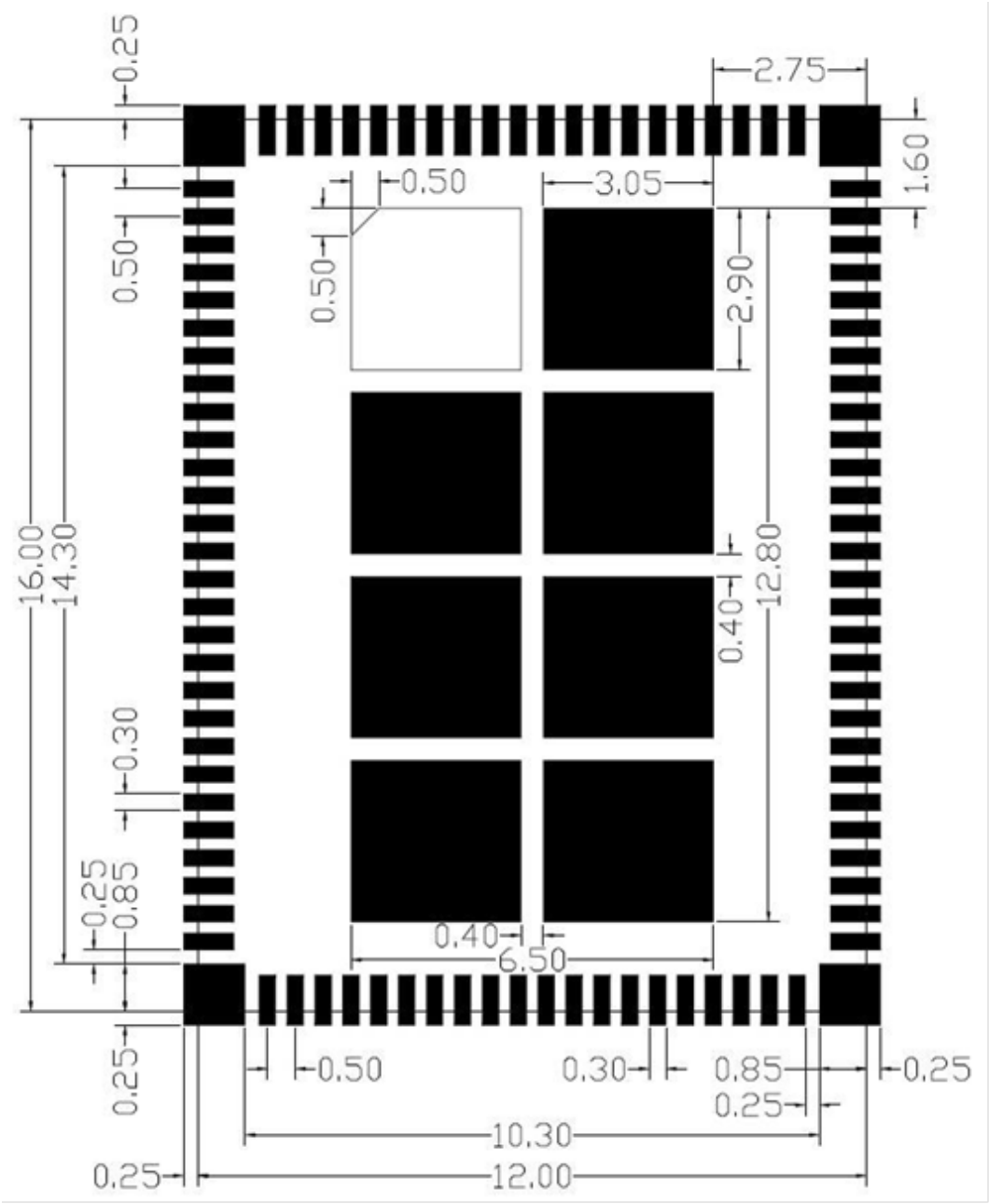
8.2 PCB Footprint

< TOP VIEW >



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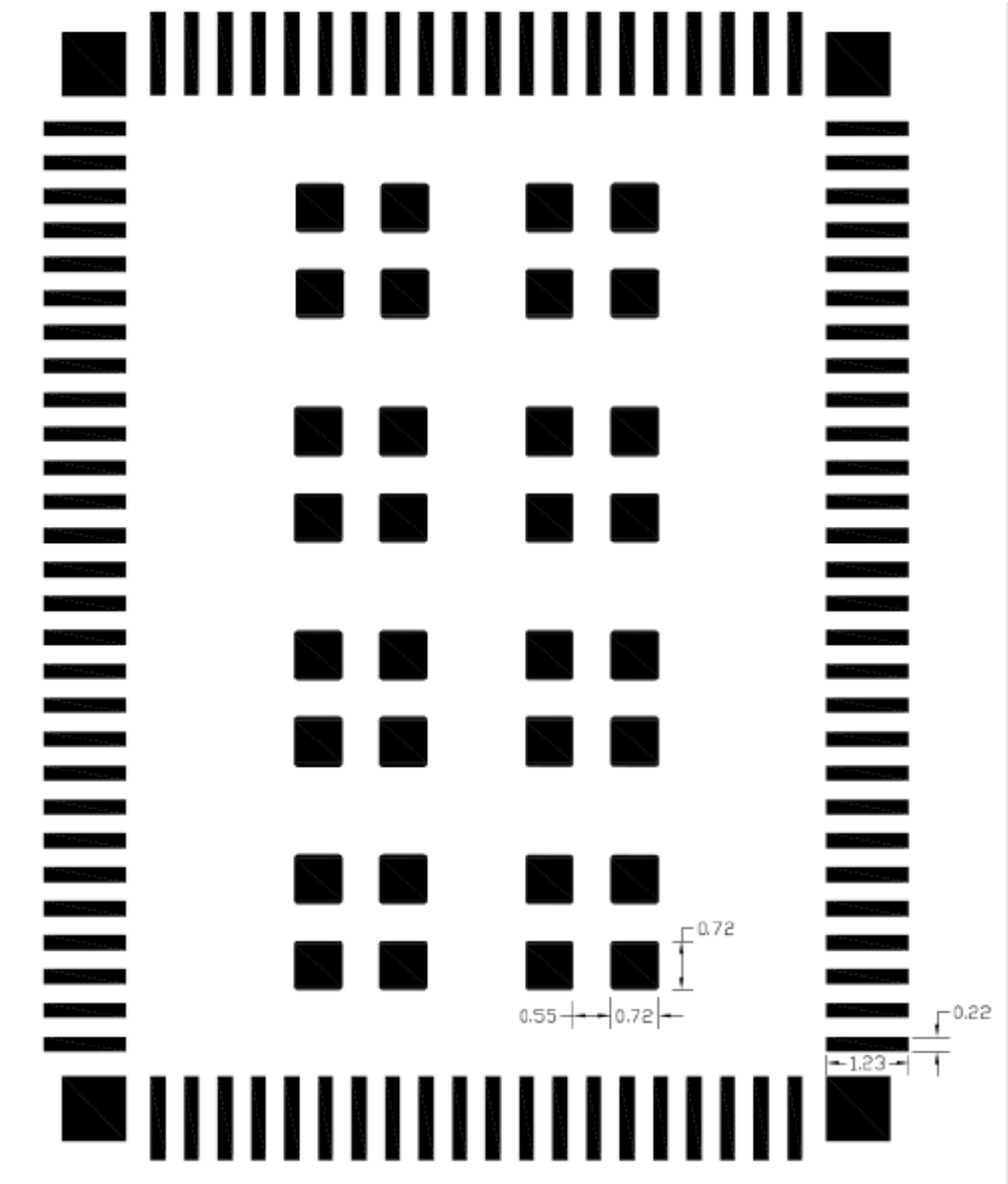
8.3 Stencil Recommendation



Unit: mm

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9. External Clock Reference

External LPO signal characteristics

Parameter	Specification	Units
Nominal input frequency	32.768	kHz
Frequency accuracy	+/-30	ppm
Duty cycle	30 - 70	%
Input signal amplitude	400 to 1800	mV, p-p
Signal type	Square-wave	-
Input impedance	>100k <5	Ω pF
Clock jitter (integrated over 300Hz – 15KHz)	<1	Hz
Output high voltage	0.7Vio - Vio	V

External Ref_CLK signal characteristics

NO	Item	Symb.	Electrical Specification				Remark
			Min	Type	Max	Units	
1	Nominal Frequency	F0		26.00000		MHz	
2	Mode of Vibration			Fundamental			
3	Frequency Tolerance	△F/F0	-10	-	10	ppm	at 25°C±3°C
4	Operating Temperature Range	T_{OPR}	-30	-	85	°C	
5	Frequency Stability	TC	-10	-	10	ppm	
6	Storage Temperature	T_{STG}	-55	-	125	°C	
7	Load capacitance	CL	-	16		pF	
8	Equivalent Series Resistance	ESR	-	-	50	Ω	
9	Drive Level	DL	-	100	200	uW	
10	Insulation Resistance	IR	500	-	-	MΩ	at 100V_{DC}
11	Shunt Capacitance	C0	-	-	3	pF	
12	Aging Per Year	Fa	-2	-	2	ppm	First Year

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9.1 SDIO Interface Description

The module supports SDIO version 2.0 for 4-bit modes (100 Mbps), and high speed 4-bit (50 MHz clocks – 200 Mbps). It has the ability to stop the SDIO clock and map the interrupt signal into a GPIO pin. This 'out-of-band' interrupt signal notifies the host when the WLAN device wants to turn on the SDIO interface. The ability to force the control of the gated clocks from within the WLAN chip is also provided.

- Function 0 Standard SDIO function (Max BlockSize / ByteCount = 32B)
- Function 1 Backplane Function to access the internal System On Chip (SOC) address space (Max BlockSize / ByteCount = 64B)
- Function 2 WLAN Function for efficient WLAN packet transfer through DMA (MaxBlock Size/ByteCount = 512B)

SDIO Pin Description

SD 4-Bit Mode	
DATA0	Data Line 0
DATA1	Data Line 1 or Interrupt
DATA2	Data Line 2 or Read Wait
DATA3	Data Line 3
CLK	Clock
CMD	Command Line

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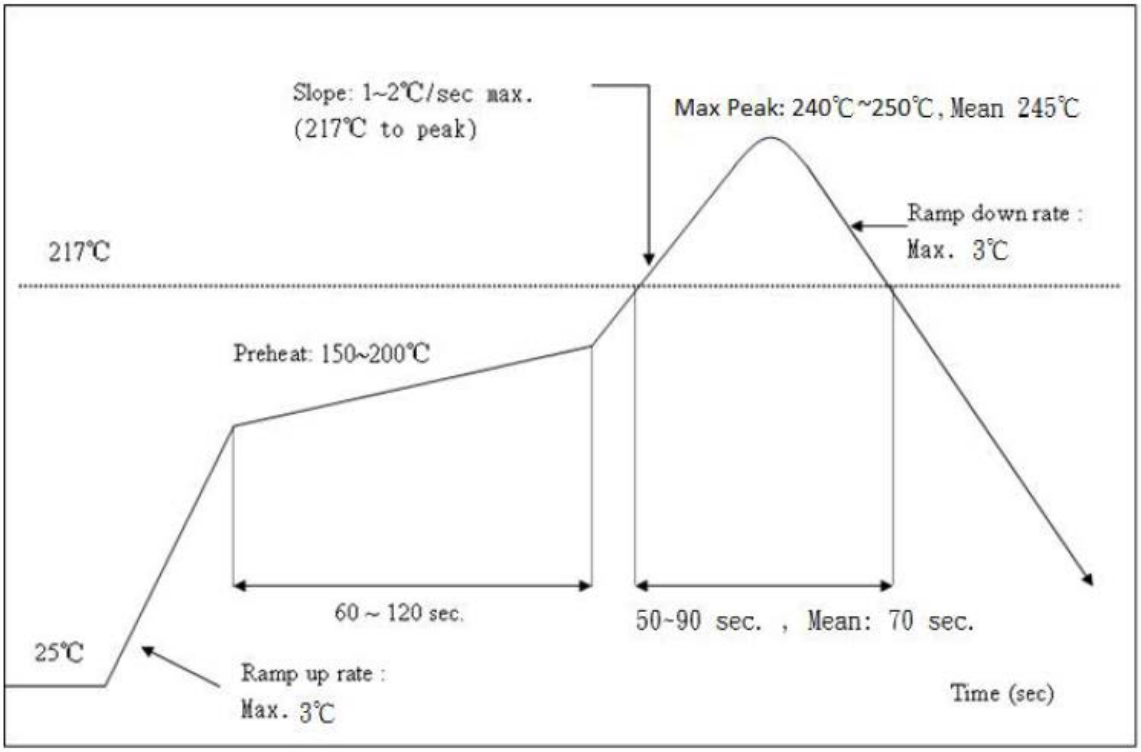
10. Recommended Reflow Profile



- Referred to IPC/JEDEC standard
- Peak Temperature : <250°C
- Cycle of Reflow: 2 times.
- The notification of WiFi module before mounting:

  The aperture of stencil should be larger than foot print of module, and the stencil thickness should be not less than 0.12mm.
- Adding Nitrogen (N2) to implement 5000ppm or less of oxygen concentration during reflow process is recommended.
- If the shelf time is exceeded, be sure baking step to remove the moisture from the component.

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10.1 Caution for SMT Preparation

Moisture Sensitivity Level: 4

1. Calculated shelf life in sealed bag: 12 months at <40℃ and <90% relative humidity (RH).

2. Peak package body temperature: 250℃.

3. After bag was opened, devices that will be subjected to reflow solder or other high temperature process must be

    a) Mounted within: 72 hours of factory conditions ≤30℃/60%RH or
    b) Stored per J-STD-033

4. Devices require bake before mounting, if:

    a) Humidity Indicator Card reads> 10% for level 2a - 5a devices or >60% for level 2 devices when read at 23±5℃
    b) 3a or 3b are not met.

5. If baking is required, refer to IPC/JEDEC J-STD-033 for bake procedure.

6. If baking is required, devices may be baked for 7 hours at 125±10℃

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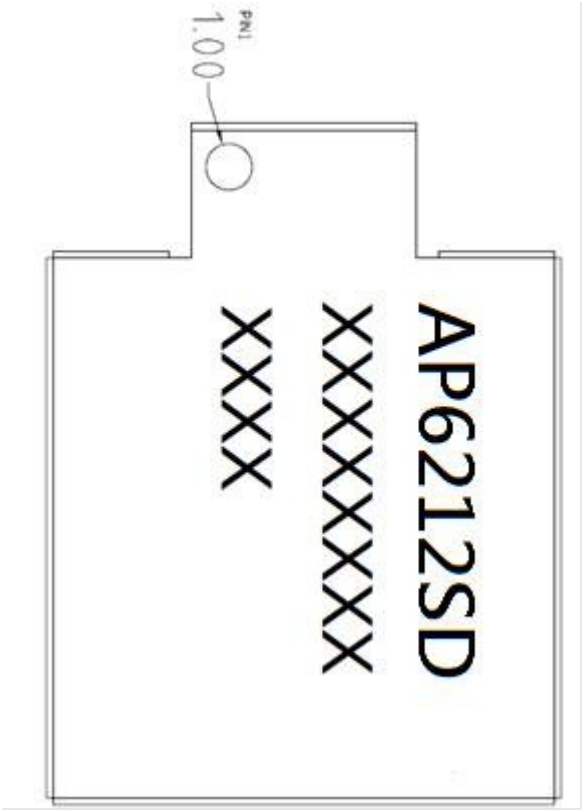
11. Package Information



- 10 sprocket hole pitch cumulative tolerance ±0.20.
- Carrier camber is within 1 mm in 250 mm.
- Material: Black Conductive Polystyrene Alloy.
- All dimensions meet EIA-481-D requirements.
- Thickness: 0.30±0.05mm.
- Component load per 13”reel : 1000 PCS

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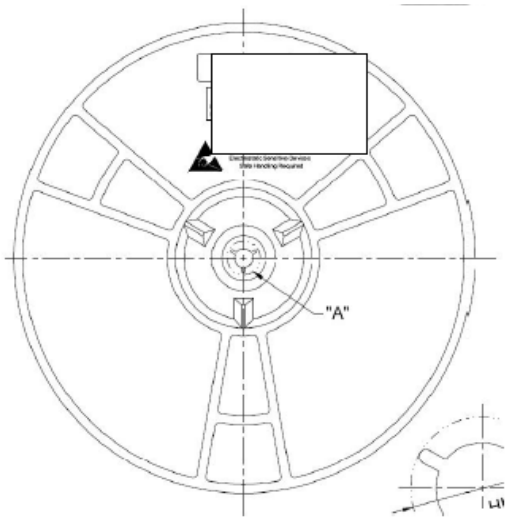

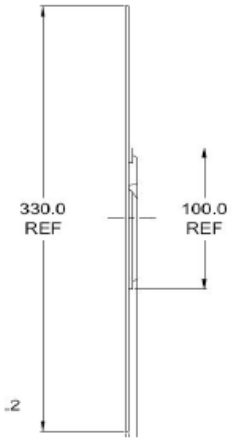

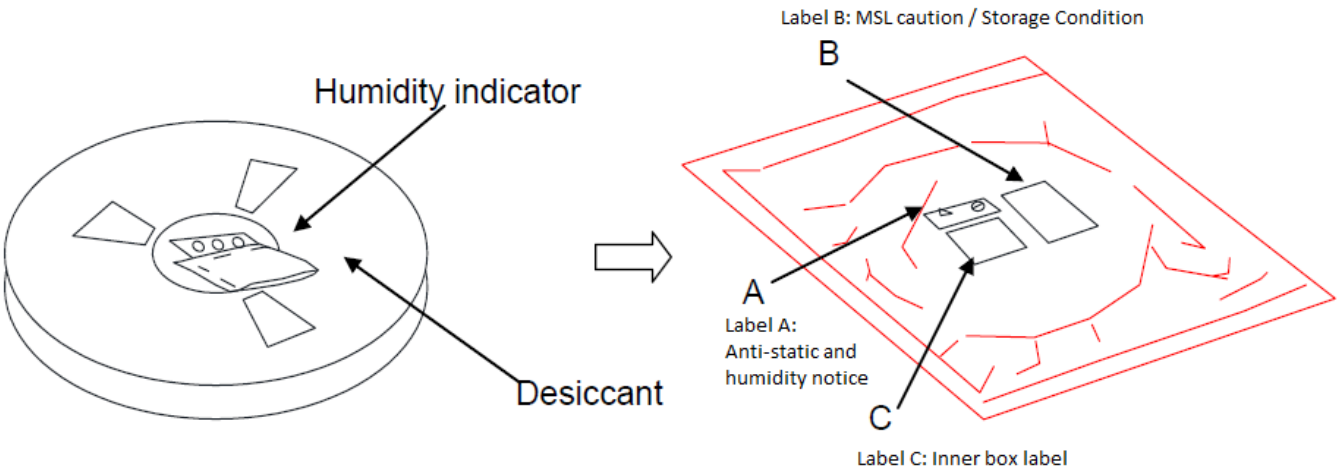

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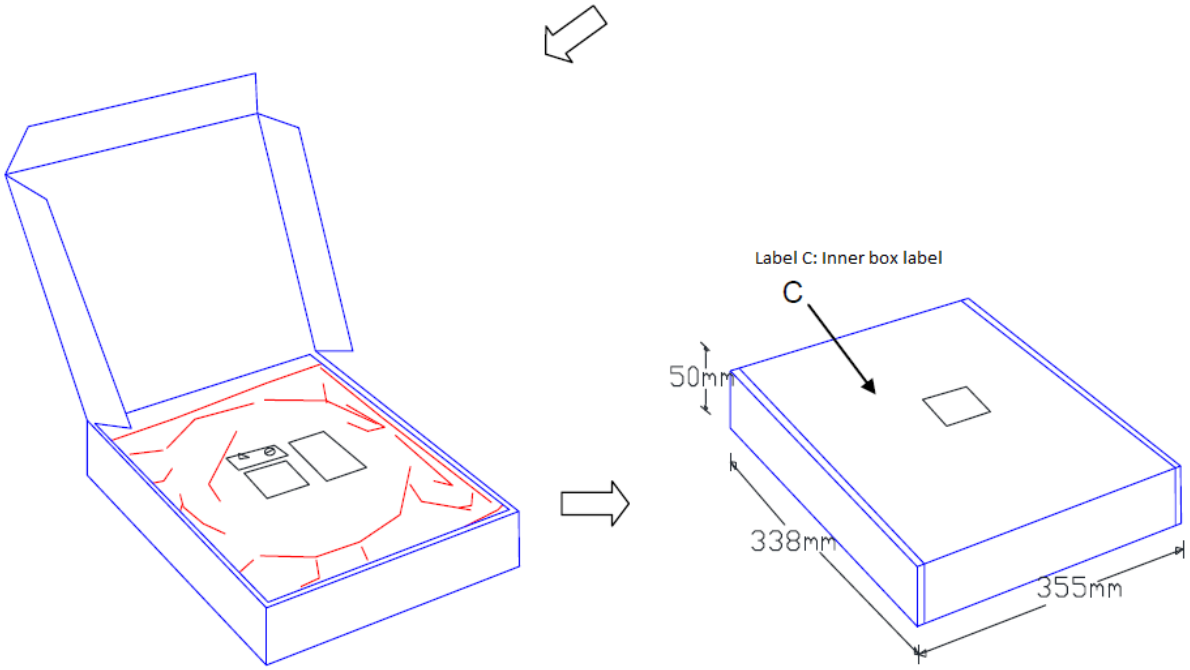

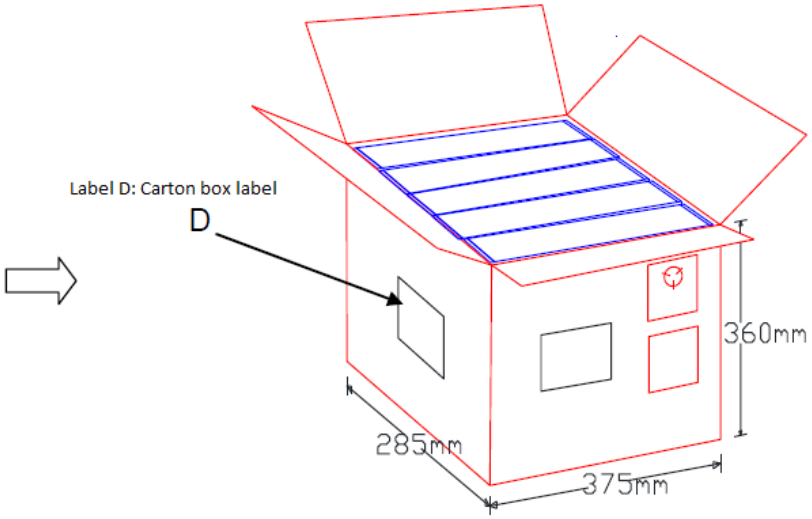

Note: 1 tape reel = 1 box = 1,000pcs
1 Carton = 5 box = 5,000pcs

12. Certification

- **FCC**
- **CE** (RED EN 300 328 V2.1.1 / EN 301 893 V2.1.1)
- **IC**
- **MIC**
- **NCC**
- **SRRC**
- **AS**
- **NZS**

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13. Ordering Information

Product Name	Part Number	Description
AP6212SD	R9701920007	11b/g/n 1T1R WiFi + BT5.2 M.2 LGA Type 1216 Module

13.1 Optional Accessory

Product Name	Part Number	Description
AD-103AG	R3410110203	Dipole Antenna, 2dBi 2.4GHz/5GHz, RP-SMA(M) connector
AD-302N	R3410110221	Dipole Antenna, 3dBi/2dBi 2.4G/5GHz, RP-SMA(M) connector
AD-303N	R3410110222	Dipole Antenna, 3dBi/3dBi 2.4G/5GHz, RP-SMA(M) connector
AD-305N	R3410110223	Dipole Antenna, 5dBi/5dBi 2.4G/5GHz, RP-SMA(M) connector
CBIRF-NE150	R3470300025	RF Cable, I-PEX/MHF4 to RP-SMA(F); L:150mm; Coaxial 0.81 Black
CBIRF-NE250	R3470300026	RF Cable, I-PEX/MHF4 to RP-SMA(F); L:250mm; Coaxial 0.81 Black

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