

Datasheet

AP6275HH3

IEEE 802.11ax/ac/a/b/g/n 2x2

WiFi with Bluetooth5.0 Combo Sip Module

The revision history of the product specification

Version	Purpose	Date	Editor
0.9	Initial Doc	2021/02/22	Aaron
0.91	Update Doc	2021/04/21	Aaron

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1. Introduction

1.1 Product Overview

SparkLAN/Ampak AP6275HH3, the first PCIe based WiFi-6 (802.11ax) module with Bluetooth technology 5.0 from Synaptic/Broadcom. This module supports DBDC (Dual Band Dual Concurrent), enable concurrent connections to multiple different frequencies (2.4GHz & 5GHz). AP6275HH3 supports full IEEE802.11 ax/ac/a/b/g/n protocol, with WiFi running PCIe (v3.0) interface, and Bluetooth through UART/PCM interface.

AP6275HH3 designed with 2 spatial streams (2T2R, or 2x2) in MU-MIMO mode. In a SiP packaging formfactor with a of 24mm x 24mm.

Software wise AP6275HH3 support Linux and Android in the near future. The module is capable to run on both x86 platform and ARM based platform, and supports STA mode and basic Soft AP Mode, recommend running on application includes: digital signage/POS, tablets, and other media consumption application (Consumer and commercial use) that requires high speed data transmission.

1.2 Product Features

1.2.1 WLAN

- Data rate of up to 1200 Mbps during single-band operation and 1430 Mbps in RSDB mode.
- 20/40/80 MHz channels for the main (Main) 2×2 WLAN core (1024-QAM modulation), and 20 MHz channels for the auxiliary (Aux) 2×2 WLAN core (256-QAM modulation).
- TX and RX low-density parity check (LDPC) support for improved range and power efficiency
- Supports PCIe v3.0 compliant and runs at Gen2 speeds.
- Zero wait dynamic frequency selection (DFS): background channel availability check (CAC) scan for immediate switch to candidate DFS channel.
- MU-MIMO

1.2.2 Bluetooth

- BT host digital interface:
 - HCI UART (up to 4 Mbps)
 - PCM for audio data
- Complies with Bluetooth Core Specification Version 5.0 with provisions for supporting future specifications. With Bluetooth Class 1 or Class 2 transmitter operation.
- Bluetooth 5 including Low-Energy Long Range (LELR).
- Supports extended synchronous connections (eSCO), for enhanced voice quality by allowing for retransmission of dropped packets
- Adaptive frequency hopping (AFH) for reducing radio frequency interference. A simplified block diagram of the module is depicted in the figure above.

2. Specification

2.1 General Specification

Standards	IEEE 802.11 ax/ac/a/b/g/n 2T2R Wi-Fi + BT 5.0 Module Bluetooth : V5.0, V4.2, V4.1, V4.0 LE, V3.0+HS, V2.1+EDR
Chipset	Synaptics
Operating Frequency	2.400 GHz ~ 2.4835 GHz (2.4GHz ISM Band) 5.150~5.850GHz (5GHz UNII Band) Bluetooth: 2.402 GHz ~ 2.480 GHz
Modulation	WiFi: 802.11b: DSSS (DBPSK, DQPSK, CCK) 802.11g: OFDM (BPSK, QPSK, 16-QAM, 64-QAM) 802.11gn: OFDM (BPSK, QPSK, 16-QAM, 64-QAM) 802.11a: OFDM (BPSK, QPSK, 16-QAM, 64-QAM) 802.11an: OFDM (BPSK, QPSK, 16-QAM, 64-QAM) 802.11ac: OFDM (BPSK, QPSK, 16-QAM, 64-QAM, 256-QAM) 802.11ax: OFDMA (BPSK, QPSK, 16-QAM, 64-QAM, 256-QAM, 1024-QAM) BT: Header: GFSK Payload 2M: $\pi/4$ -DQPSK Payload 3M: 8-DPSK
WiFi Interface	Support PCIe v3.0 compliant and runs at Gen2 speeds.
BT Interface	UART / PCM
Form Factor	SiP (System in Package) Stamp Type
Antenna	External
Dimension	L x W x H: 24mm(\pm 0.15mm) x 24mm(\pm 0.15mm) x 2.1mm(Max.)
Operating temperature	-30°C to 85°C
Storage temperature	-40°C to 85°C
Humidity(Non-Condensing)	10% ~ 95% (Operating)
Weight	TBD
Driver Support	Linux, Android

Note: The optimal RF performance specified in the data sheet, however, is guaranteed only -10 °C to +55 °C and 3.2V < VBAT < 3.6V without derating performance.

2.2 WiFi 2.4GHz RF Specification

Conditions: VBAT=3.3V; VDDIO=1.8V; Temp:25°C

Output Power, tolerance $\pm 1.5\text{dB}$					
The transmit EVM quality & spectrum mask are compliant with IEEE 802.11 standard					
802.11b	1Mbps	2Mbps	5.5Mbps	11Mbps	
	19	19	19	19	
802.11g	6、9Mbps	12、18Mbps	24Mbps	36Mbps	48Mbps
	18.5	18	18	18	18
	54Mbps				
	17				
802.11n 20MHz	MCS0~2	MCS3	MCS4	MCS5	MCS6
	18.5	18	18	18	17
	MCS7				
	16.5				
802.11ax 20MHz	HE0~2	HE3	HE4	HE5	HE6
	18.5	18	18	18	17
	HE7	HE8	HE9		
	16.5	16	15		

Note: The specifications of RF output power are subject to change to fulfill the safety regulation and requirements in end-user product.

Sensitivity, tolerance $\pm 2\text{ dB}$				
CCK modulation PER $\leq 8\%$ 、OFDM modulation PER $\leq 10\%$				
802.11b	Data Rate	Spec.(dBm)		
	1Mbps	-97		
	2Mbps	-95		
	5.5Mbps	-93		
	11Mbps	-90		
802.11g SISO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	6Mbps	-94	24Mbps	-85
	9Mbps	-92	36Mbps	-83
	12Mbps	-91	48Mbps	-78
	18Mbps	-89	54Mbps	-77
802.11g MIMO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	6Mbps	-96	24Mbps	-88
	9Mbps	-94	36Mbps	-85
	12Mbps	-93	48Mbps	-80
	18Mbps	-91	54Mbps	-79
802.11n_20MHz SISO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0	-93	MCS4	-82.5
	MCS1	-90	MCS5	-80
	MCS2	-88	MCS6	-77
	MCS3	-85	MCS7	-76

802.11n_20MHz MIMO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0	-95	MCS5	-82
	MCS1	-92	MCS6	-79
	MCS2	-90	MCS7	-78
	MCS3	-87	MCS8	-94
	MCS4	-84.5	MCS15	-75
802.11ax_20MHz SISO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0	-94	MCS6	-77
	MCS1	-90	MCS7	-77
	MCS2	-88	MCS8	-73
	MCS3	-85	MCS9	-71
	MCS4	-82.5		
	MCS5	-80		
Maximum Input Level	802.11b : -10 dBm			
	802.11g/n/ax : -20 dBm			

2.3 WiFi 5GHz RF Specification

Conditions : VBAT=3.3V ; VDDIO=1.8V ; Temp:25°C

Output Power , tolerance ± 2 dB					
The transmit EVM quality & spectrum mask are compliant with IEEE 802.11 standard					
802.11a	Frequency (MHz)	6~9Mbps	12~18Mbps	24Mbps	36Mbps
	5150~5350	18.5	18.5	18.5	18.5
	5470~5720	18.5	18.5	18.5	18.5
	5725~5845	18.5	18.5	18.5	18.5
	Frequency (MHz)	48Mbps	54Mbps		
	5150~5350	18.5	17.5		
	5470~5720	18.5	17.5		
	5725~5845	18.5	17.5		
802.11n 20MHz	Frequency (MHz)	MCS0~2	MCS3	MCS4	MCS5
	5150~5350	18.5	18.5	18.5	18.5
	5470~5720	18.5	18.5	18.5	18.5
	5725~5845	18.5	18.5	18.5	18.5
	Frequency (MHz)	MCS6	MCS7		
	5150~5350	17.5	16		
	5470~5720	17.5	16		
	5725~5845	17.5	16		

802.11n 40MHz	Frequency (MHz)	MCS0~2	MCS3	MCS4	MCS5
	5150~5350	18.5	18.5	18	18
	5470~5720	18.5	18.5	18	18
	5725~5845	18.5	18.5	18	18
	Frequency (MHz)	MCS6	MCS7		
	5150~5350	17	16		
	5470~5720	17	16		
5725~5845	17	16			
802.11ac 20MHz	Frequency (MHz)	MCS0~2	MCS3	MCS4	MCS5
	5150~5350	18.5	18.5	18.5	18.5
	5470~5720	18.5	18.5	18.5	18.5
	5725~5845	18.5	18.5	18.5	18.5
	Frequency (MHz)	MCS6	MCS7	MCS8	
	5150~5350	17.5	16	15	
	5470~5720	17.5	16	15	
5725~5845	17.5	16	15		
802.11ac 40MHz	Frequency (MHz)	MCS0~2	MCS3	MCS4	MCS5
	5150~5350	18.5	18.5	18.5	18.5
	5470~5720	18.5	18.5	18.5	18.5
	5725~5845	18.5	18.5	18.5	18.5
	Frequency (MHz)	MCS6	MCS7	MCS8	MCS9
	5150~5350	17.5	16	15	14
	5470~5720	17.5	16	15	14
5725~5845	17.5	16	15	14	
802.11ac 80MHz	Frequency (MHz)	MCS0~2	MCS3	MCS4	MCS5
	5150~5350	18	18	17.5	17.5
	5470~5720	18	18	17.5	17.5
	5725~5845	18	18	17.5	17.5
	Frequency (MHz)	MCS6	MCS7	MCS8	MCS9
	5150~5350	16.5	15.5	15	14
	5470~5720	16.5	15.5	15	14
5725~5845	16.5	15.5	15	14	
802.11ax 20MHz	Frequency (MHz)	MCS0~2	MCS3	MCS4	MCS5
	5150~5350	18.5	18.5	18.5	18.5
	5470~5720	18.5	18.5	18.5	18.5
	5725~5845	18.5	18.5	18.5	18.5
	Frequency (MHz)	MCS6	MCS7	MCS8	MCS9
	5150~5350	17.5	16	15	14
	5470~5720	17.5	16	15	14
	5725~5845	17.5	16	15	14
	Frequency (MHz)	MCS10	MCS11		
	5150~5350	13	13		
	5470~5720	13	13		
5725~5845	13	13			

802.11ax 40MHz	Frequency (MHz)	MCS0~2	MCS3	MCS4	MCS5
	5150~5350	18.5	18.5	18.5	18.5
	5470~5720	18.5	18.5	18.5	18.5
	5725~5845	18.5	18.5	18.5	18.5
	Frequency (MHz)	MCS6	MCS7	MCS8	MCS9
	5150~5350	17.5	16	15	14
	5470~5720	17.5	16	15	14
	5725~5845	17.5	16	15	14
	Frequency (MHz)	MCS10	MCS11		
	5150~5350	13	13		
5470~5720	13	13			
5725~5845	13	13			
802.11ax 80MHz	Frequency (MHz)	MCS0~2	MCS3	MCS4	MCS5
	5150~5350	18	18	17.5	17.5
	5470~5720	18	18	17.5	17.5
	5725~5845	18	18	17.5	17.5
	Frequency (MHz)	MCS6	MCS7	MCS8	MCS9
	5150~5350	16.5	15.5	15	14
	5470~5720	16.5	15.5	15	14
	5725~5845	16.5	15.5	15	14
	Frequency (MHz)	MCS10	MCS11		
	5150~5350	13	13		
5470~5720	13	13			
5725~5845	13	13			

Note: The specifications of RF output power are subject to change to fulfill the safety regulation and requirements in end-user product.

Sensitivity, tolerance ± 1.5 dB

CCK modulation PER $\leq 8\%$ 、OFDM modulation PER $\leq 10\%$

802.11a SISO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	6Mbps	-94	24Mbps	-85
	9Mbps	-92	36Mbps	-82
	12Mbps	-91	48Mbps	-78
	18Mbps	-88	54Mbps	-76
802.11a MIMO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	6Mbps	-96	24Mbps	-87
	9Mbps	-94	36Mbps	-85
	12Mbps	-93	48Mbps	-80
	18Mbps	-90	54Mbps	-78
802.11n_20MHz SISO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0	-93	MCS4	-82
	MCS1	-91	MCS5	-77
	MCS2	-89	MCS6	-76
	MCS3	-85	MCS7	-74

802.11n_20MHz MIMO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0	-95	MCS5	-79
	MCS1	-93	MCS6	-78
	MCS2	-91	MCS7	-76
	MCS3	-87	MCS8	-93
	MCS4	-84	MCS15	-74
802.11n_40MHz SISO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0	-91	MCS4	-79
	MCS1	-88	MCS5	-75
	MCS2	-86	MCS6	-73
802.11n_40MHz MIMO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0	-93	MCS5	-77
	MCS1	-90	MCS6	-75
	MCS2	-88	MCS7	-73
	MCS3	-84	MCS8	-91
	MCS4	-81	MCS15	-71
802.11ac_20MHz SISO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0	-93	MCS5	-77
	MCS1	-91	MCS6	-76
	MCS2	-89	MCS7	-74
	MCS3	-85	MCS8	-73
802.11ac_20MHz MIMO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0,NSS=1	-95	MCS6,NSS=1	-78
	MCS1,NSS=1	-93	MCS7,NSS=1	-76
	MCS2,NSS=1	-92	MCS8,NSS=1	-75
	MCS3,NSS=1	-87	MCS0,NSS=2	-93
	MCS4,NSS=1	-84	MCS8,NSS=2	-70
802.11ac_40MHz SISO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0	-91	MCS5	-75
	MCS1	-88	MCS6	-73
	MCS2	-86	MCS7	-71
	MCS3	-82	MCS8	-70
802.11ac_40MHz MIMO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0,NSS=1	-93	MCS6,NSS=1	-75
	MCS1,NSS=1	-90	MCS7,NSS=1	-73
	MCS2,NSS=1	-88	MCS8,NSS=1	-72
	MCS3,NSS=1	-84	MCS9,NSS=1	-70.5
	MCS4,NSS=1	-81	MCS0,NSS=2	-91
802.11ac_40MHz MIMO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0,NSS=1	-93	MCS6,NSS=1	-75
	MCS1,NSS=1	-90	MCS7,NSS=1	-73
	MCS2,NSS=1	-88	MCS8,NSS=1	-72
	MCS3,NSS=1	-84	MCS9,NSS=1	-70.5
	MCS4,NSS=1	-81	MCS0,NSS=2	-91
802.11ac_40MHz MIMO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0,NSS=1	-93	MCS6,NSS=1	-75
	MCS1,NSS=1	-90	MCS7,NSS=1	-73
	MCS2,NSS=1	-88	MCS8,NSS=1	-72
	MCS3,NSS=1	-84	MCS9,NSS=1	-70.5
	MCS4,NSS=1	-81	MCS0,NSS=2	-91
802.11ac_40MHz MIMO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0,NSS=1	-93	MCS6,NSS=1	-75
	MCS1,NSS=1	-90	MCS7,NSS=1	-73
	MCS2,NSS=1	-88	MCS8,NSS=1	-72
	MCS3,NSS=1	-84	MCS9,NSS=1	-70.5
	MCS4,NSS=1	-81	MCS0,NSS=2	-91

802.11ac_80MHz SISO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0	-88	MCS5	-72
	MCS1	-85	MCS6	-70
	MCS2	-83	MCS7	-68
	MCS3	-79	MCS8	-67
	MCS4	-76	MCS9	-66
802.11ac_80MHz MIMO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0,NSS=1	-90	MCS6,NSS=1	-72
	MCS1,NSS=1	-87	MCS7,NSS=1	-70
	MCS2,NSS=1	-85	MCS8,NSS=1	-69
	MCS3,NSS=1	-81	MCS9,NSS=1	-67
	MCS4,NSS=1	-78	MCS0,NSS=2	-88
	MCS5,NSS=1	-71	MCS9,NSS=2	-64
802.11ax_20MHz SISO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0	-93	MCS6	-76
	MCS1	-91	MCS7	-73
	MCS2	-89	MCS8	-71
	MCS3	-86	MCS9	-67
	MCS4	-82	MCS10	-62
	MCS5	-78	MCS11	-60
802.11ax_40MHz SISO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0	-88	MCS6	-70
	MCS1	-86	MCS7	-69
	MCS2	-83	MCS8	-65
	MCS3	-80	MCS9	-64
	MCS4	-76	MCS10	-60
	MCS5	-72	MCS11	-55
802.11ax_80MHz SISO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0	-88	MCS6	-70
	MCS1	-85	MCS7	-68
	MCS2	-82	MCS8	-65
	MCS3	-79	MCS9	-64
	MCS4	-76	MCS10	-58
	MCS5	-71	MCS11	-54
Maximum Input Level	802.11a/n/ac : -30 dBm			

2.4 Bluetooth RF Specification

Conditions: VBAT=3.3v ; VDDIO=1.8V ; Temp:25°C

RF Specification	
Output Power , tolerance ± 1.5 dB	
	CL1 (dBm)
BDR Output Power	8
EDR Output Power	6
BLE Output Power	7
Sensitivity, tolerance ± 1.5 dB	
Sensitivity @ BER=0.1% for GFSK (1Mbps)	-89 dBm
Sensitivity @ BER=0.01% for $\pi/4$ -DQPSK (2Mbps)	-92 dBm
Sensitivity @ BER=0.01% for 8DPSK (3Mbps)	-84 dBm
Sensitivity @ BER=30.8% for LE (1Mbps)	-92 dBm
Sensitivity @ BER=30.8% for 2LE (2Mbps)	-91 dBm
Maximum Input Level	GFSK (1Mbps):-20dBm
	$\pi/4$ -DQPSK (2Mbps) :-20dBm
	8DPSK (3Mbps) :-20dBm

Note* : The Bluetooth BDR output power is able to be configured by firmware (hcd file).

3. Electrical Characteristics

3.1 Absolute Maximum Ratings

Symbol	Description	Min.	Max.	Unit
VBAT	IC Input supply Voltage	-0.5	5	V
VDDIO	Digital/Bluetooth/SDIO/ I/O Voltage	-0.5	2.07	V
VBATFEM	FEM Input supply Voltage	-0.5	5	V

Extreme caution must be exercised to prevent electrostatic discharge (ESD) damage.

Symbol	Condition	Minimum ESD Rating	Unit
ESD_HAND_HBM	Human body model contact discharge per JEDEC EID/JESD22-A114	2	kV
ESD_HAND_CDM	Charged device model contact discharge per JEDEC EIA/JESD22-C101	250	V

Note: All pins except O_PAD_BT_13DBMOP, which passed at 250V.

3.2 Recommended Operating Rating

The module requires two power supplies: VBAT and VDDIO.

Voltage rails	Min.	Typ.	Max.	Unit
VBAT	3.2	3.3	3.8	V
VBATFEM	3.2	3.3	4.6	V
VDDIO	1.68	1.8	1.98	V

VBAT current consumption 1200mA(Peak), when VBAT = 3.3V

The module requires two power supplies: other Digital I/O Pins.

For VDDIO=1.8V	Min.	Max.	Unit
VIH	0.65×VDDIO	N/A	V
VIL	N/A	0.4×VDDIO	V
VOH output@2mA	VDDIO-0.4	N/A	V
VOL output@2mA	N/A	0.4	V

4. Host Interface Timing Diagram

4.1 Power-up Sequence Timing Diagram

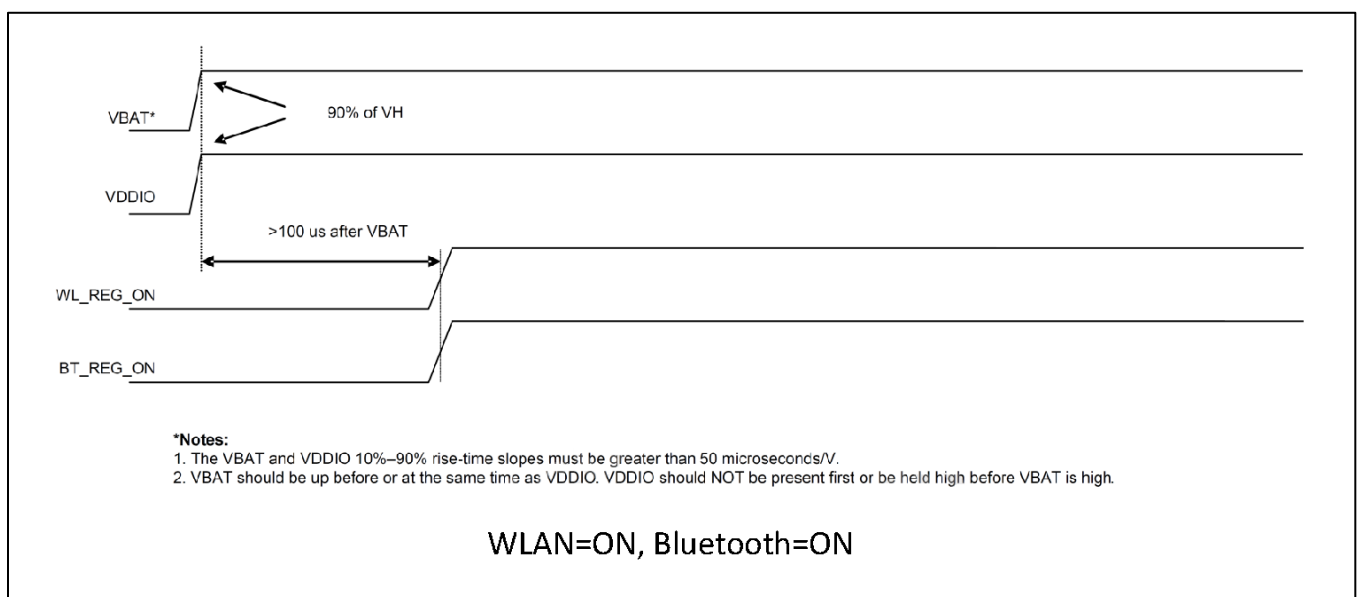
The module has two signals that allow the host to control power consumption by enabling or disabling the Bluetooth, WLAN and internal regulator blocks. These signals are described below. Additionally, diagrams are provided to indicate proper sequencing of the signals for various operating states. The timing value indicated are minimum required values; longer delays are also acceptable.

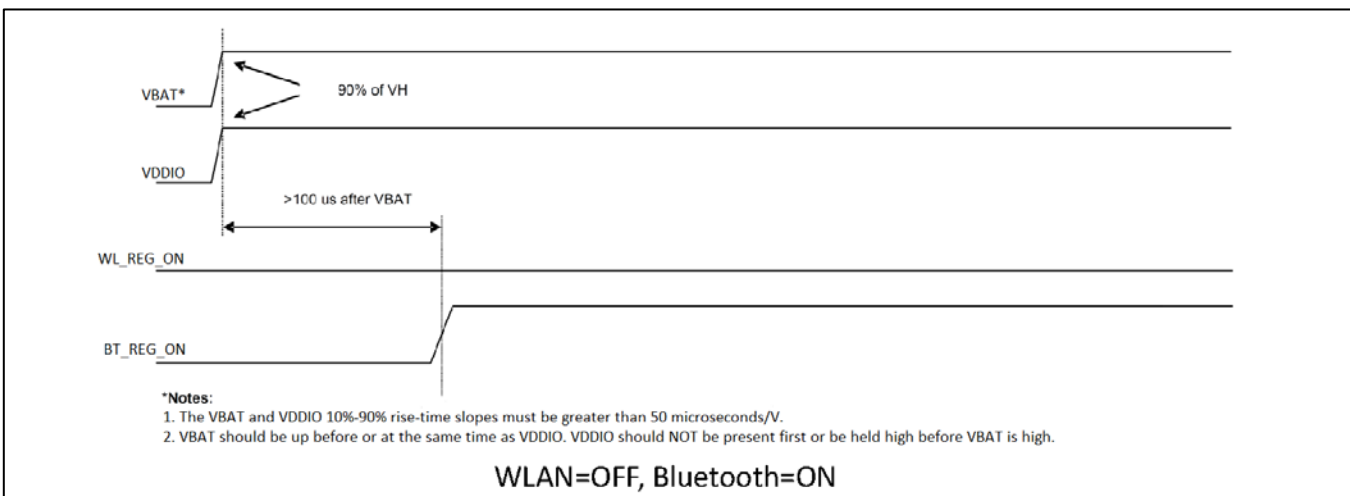
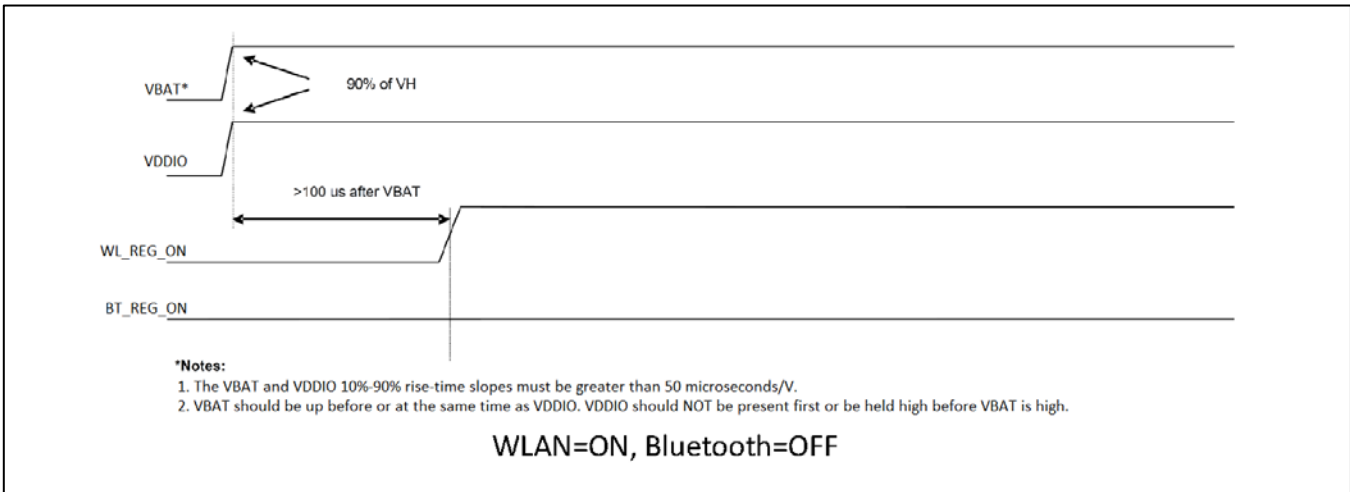
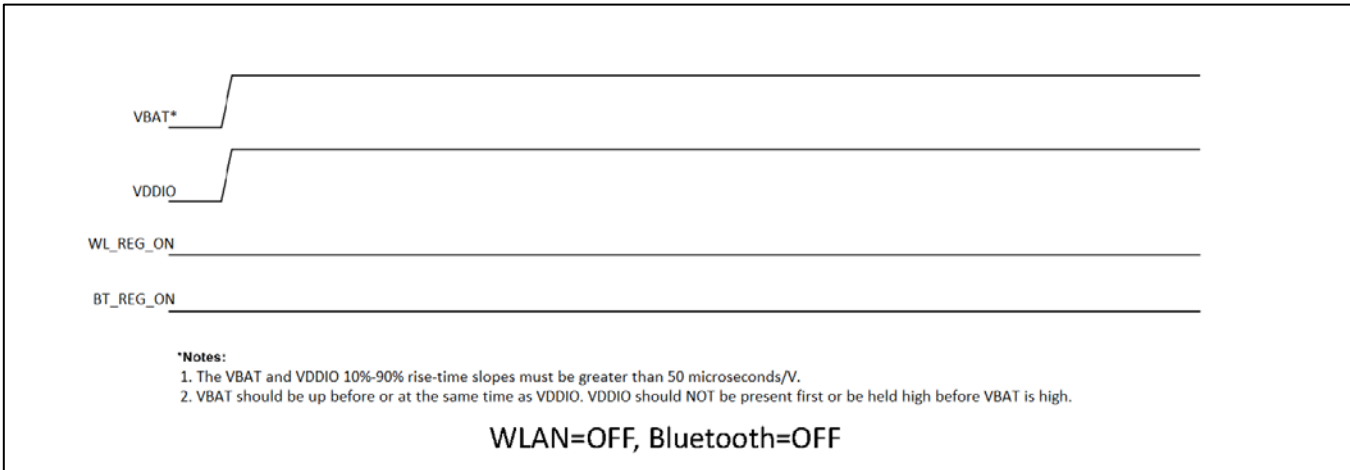
- WL_REG_ON:** This signal is used by the PMU to power up the WLAN section. It is also OR-gated with the BT_REG_ON input to control the internal regulators. When this pin is high, the regulators are enabled and the WLAN section is out of reset. When this pin is low, the WLAN section is in reset. If BT_REG_ON and WL_REG_ON are both low, the regulators are disabled. This pin has an internal 50kΩ pull-down resistor.
- BT_REG_ON:** This signal is used by the PMU to decide whether or not to power down the internal regulators. If BT_REG_ON and WL_REG_ON are low, the regulators will be disabled. This pin has an internal 50 kΩ pull-down resistor.

NOTE: 1. The VBAT and VDDIO 10%–90% rise time slopes must be greater than 50 μs/V.

2. The module main chip has an internal power-on reset (POR) circuit. The device will be held in reset for a maximum of 110 ms after VDDC and VDDIO have both passed the POR threshold.

Wait at least 150 ms after VDDC and VDDIO are available before initiating PCIe accesses.





4.2 PCIe Interface Description

The PCI Express(Pcie) core on the AP6275HH3 is a high-performance serial I/O interconnect that is protocol compliant and electrically compatible with the PCI Express Base Specification v3.0 running at Gen2 speeds.

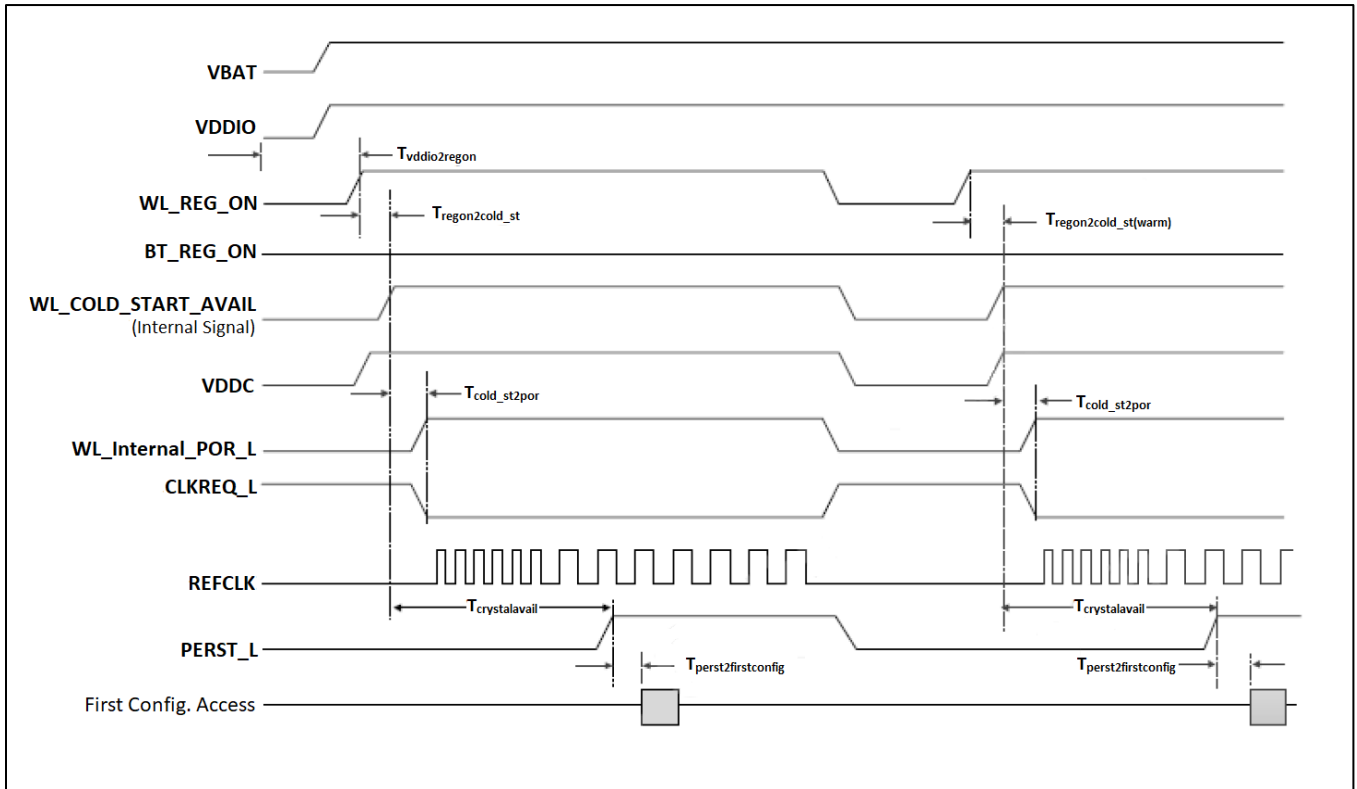
PCI Express Interface Parameters

Parameter	Symbol	Comments	Min.	Typ.	Max.	Unit
General^a						
Baud	BPS	-	-	5	-	Gbaud
Reference clock peak - peak differential	Vref	LVPECL,AC coupled	0.95	-	-	V
Receiver						
Differential termination	ZRX-DIFF-DC	Differential termination	80	100	120	Ω
DC impedance	ZRX-DC	DC common-mode impedance	40	50	60	Ω
Powered down termination (POS)	ZRX-HIGH-IMP-DC-POS	Powered down or RESET high impedance	100k	-	-	Ω
Powered down termination (NEG)	ZRX-HIGH-IMP-DC-NEG	Powered down or RESET high impedance	1k	-	-	Ω
Input voltage	VRX-DIFFp-p	AC copled, differential p-p	175	-	-	mV
Jitter tolerance	TRX-EVE	Minimum receiver eye width	0.4	--	-	UI
Differential return loss	RLRX-DIFF	Differential return loss	10	-	-	dB
Common-mode return loss	RLRX-CM	Common-mode return loss	6	-	-	dB
Unexpected electrical idle enter detect threshold integration time	TRX-IDEL-DET-DIFF-ENTERTIME	An Unexpected electrical idle must be recognized no longer than this time to signal an unexpected idle condition	-	-	10	ms
Signal detect threshold	VRX-IDLE-DET-DIFFp-p	Electrical idle detect threshold	65	-	175	mV
Transmitter						
Output voltage	VTX-DIFFp-p	Differential p-p, detect threshold	0.8	-	1200	mV
Output voltage rise time	VTX-RISE	20% to 80%	0.125 (2.5 GT/s) 0.15 (5 GT/s)	-	-	UI
Output voltage fall time	VTX-FALL	80% to 20%	0.125 (2.5 GT/s) 0.15 (5 GT/s)	-	-	UI
RX detection voltage swing	VTX-RCV-DETECT	The amount of voltage change allowed during receiver detection	-	-	600	mV

PCI Express Interface Parameters(Continued)

Parameter	Symbol	Comments	Min.	Typ.	Max.	Unit
TX AC peak common-mode voltage (5 GT/s)	VTX-CM-AC-PP	TX AC common-mode voltage (5 GT/s)	-	-	100	mV
TX AC peak common-mode voltage (2.5 GT/s)	VTX-CM-AC-P	TX AC common-mode voltage (2.5 GT/s)	-	-	20	mV
Absolute delta of DC common-mode voltage during L0 and electrical idle	VTX-CM-DC-ACTIVE-DLE-DELTA	Absolute delta of DC common-mode voltage during L0 and electrical idle	0	-	100	mV
Absolute delta of DC common-mode voltage between D+ and D-	VTX-CM-DC-LINE-DELTA	DC offset between D+ and D-	0	-	25	mV
Electrical idle differential peak output voltage	VTX-IDLE-DIFF-AC-p	Peak-to-peak voltage	0	-	20	mV
TX short circuit current	ITX-SHORT	Current limit when TX output is shorted to ground	-	-	90	mA
DC differential TX termination	ZTX-DIFF-DC	Low impedance defined during signaling (parameter is captured for 5.0 GHz by RLTX-DIFF)	80	-	120	Ω
Differential return loss	RLTX-DIFF	Differential return loss	10 (min) for 0.05: 1.25 GHz	-	-	dB
Common-mode return loss	RLTX-CM	Common-mode return loss	6	-	-	dB
TX eye width	TTX-EYE	Minimum TX eye width	0.75	-	-	UI

4.3 WLAN/PCIe Power-up timing



Timing Parameter	Notes	Value ^a	Unit
T _{vddio2regon}	-	0.1	ms
T _{regon2cold_st}	3.4 ms+162 instruction-level parallelism(ILP) cycles	10.13	ms
T _{cold_st2por}	54 ILP cycles	2.24	ms
T _{crystalavail}	509 ILP cycles	21.17	ms
T _{perst2firstconfig}	-	6.0	ms
T _{vddioon2firstconfig}	T _{vddio2regon} +T _{regon2cold_st} +T _{crystalavail} +T _{perst2firstconfig}	37.4 ^b	ms
T _{regon2cold_st(warm)}	162 ILP cycles	6.73	ms

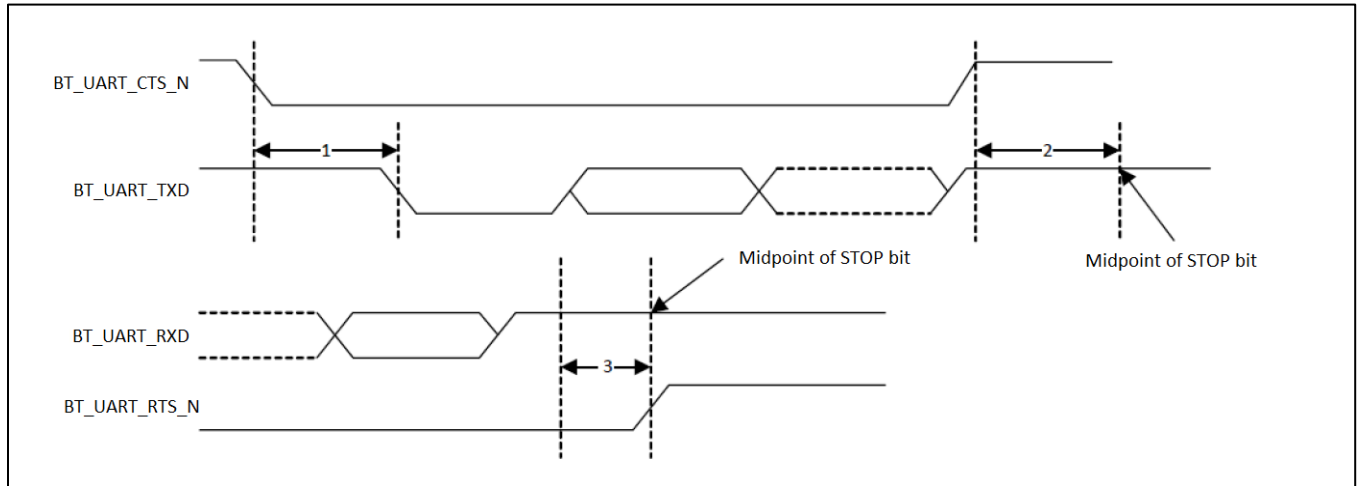
a. The time values assume an ILP tolerance ±30%

b. With VDDIO as a reference, 37.4 ms is the minimum system wait time before issuing the first configuration access

4.4 UART Interface Description

The AP6275HH3 UART is a standard 4-wire interface with adjustable baud rates from 9600 bps to 4.0 Mbps. The interface features an automatic baud rate detection capability that returns a baud rate selection. Alternatively, the baud rate may be selected through a vendor-specific UART HCI command.

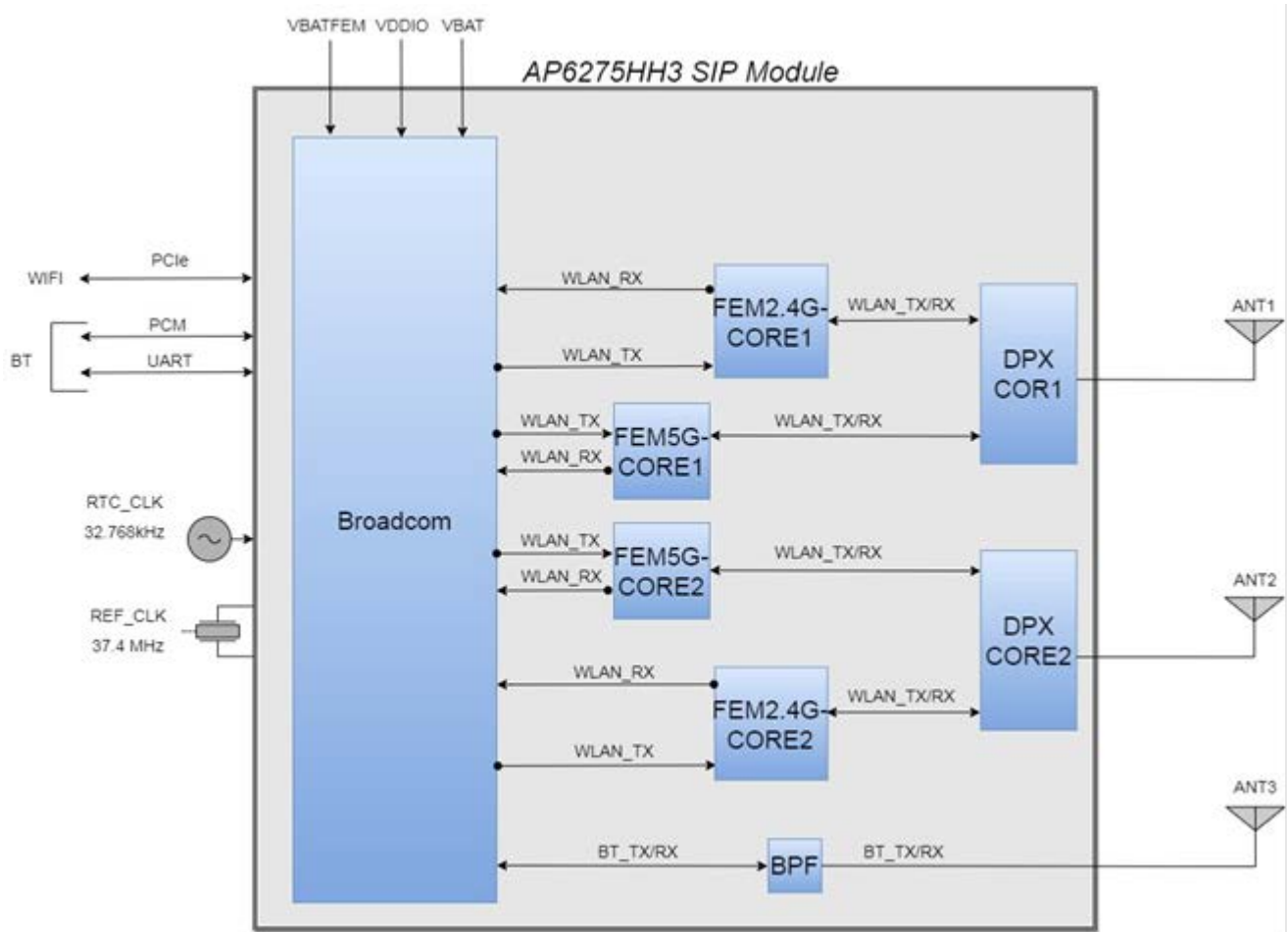
UART Timing



UART Timing Specifications

Ref	Characteristics	Min.	Typ.	Max.	Unit
1	Delay time, BT_UART_CTS_N low BT_UART_TXD valid	-	-	1.5	Bit periods
2	Setup time, BT_UART_CTS_N high before midpoint stop bit	-	-	0.5	Bit periods
3	Delay time, midpoint of stop bit BT_UART_RTS_N high	-	-	0.5	Bit periods

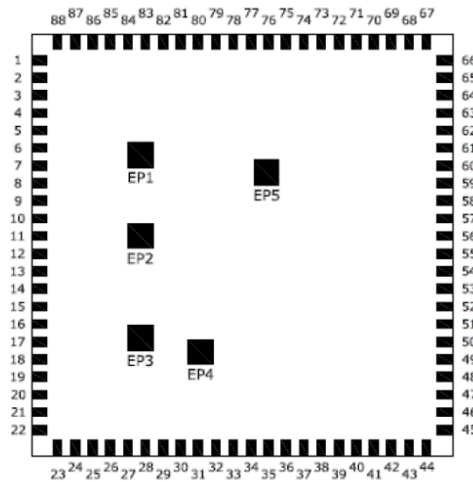
5. Block Diagram



6. Pin Definition

6.1 Pin Outline

PIN OUTLINE
<TOP VIEW>



6.2 Pin Table

NO	Name	Type	Description
1	GND	G	Ground connections
2	GND	G	Ground connections
3	WL_ANT0	I/O	RF I/O port0
4	GND	G	Ground connections
5	GND	G	Ground connections
6	GND	G	Ground connections
7	GND	G	Ground connections
8	GND	G	Ground connections
9	GND	G	Ground connections
10	GND	G	Ground connections
11	GND	G	Ground connections
12	GND	G	Ground connections
13	GND	G	Ground connections
14	GND	G	Ground connections
15	GND	G	Ground connections
16	GND	G	Ground connections
17	GND	G	Ground connections

18	GND	G	Ground connections
19	GND	G	Ground connections
20	WL_ANT1	I/O	RF I/O port1
21	GND	G	Ground connections
22	GND	G	Ground connections
23	GND	G	Ground connections
24	VBATFEM	P	FEM power voltage source input
25	VBATFEM	P	FEM power voltage source input
26	WL_GPIO_2	I/O	WL_GPIO_2
27	WL_REG_ON	I	Low asserting reset for WiFi core
28	WL_DVE_WAKE	O	HOST to wake-up WLAN and WL_GPIO_1
29	WL_HOST_WAKE	O	WLAN to wake-up HOST and WL_GPIO_0
30	GND	G	Ground connections
31	WL_GPIO_7	I/O	WL_GPIO_7
32	WL_GPIO_6	I/O	WL_GPIO_6
33	WL_GPIO_3	I/O	WL_GPIO_3
34	NC	-	Floating (Don't connected to ground)
35	NC	-	Floating (Don't connected to ground)
36	WL_UART_CTS_N	I	WIFI Debug UART interface
37	WL_UART_RTS_N	O	WIFI Debug UART interface
38	WL_UART_RXD	I	WIFI Debug UART interface
39	WL_UART_TXD	O	WIFI Debug UART interface
40	CLK_REQ	I/O	Reference clock request(shared BT and WIFI) if not used, this can be no-connect
41	PCIE_PREST_L	I	PCIe host indication to reset the device
42	PCIE_PME_L	OD	PCIe power management event output
43	PCIE_CLKREQ_L	OD	PCIe clock request
44	GND	G	Ground connections
45	ABUCK_1P12	I	Internal Analog Buck voltage generation pin
46	ASR_VLX	O	Internal Analog Buck voltage generation pin
47	GND	G	Ground connections
48	CSR_VLX	O	Internal Buck voltage generation pin
49	GND	G	Ground connections
50	CBUCK_0P9	I	Internal Buck voltage generation pin
51	GND	G	Ground connections

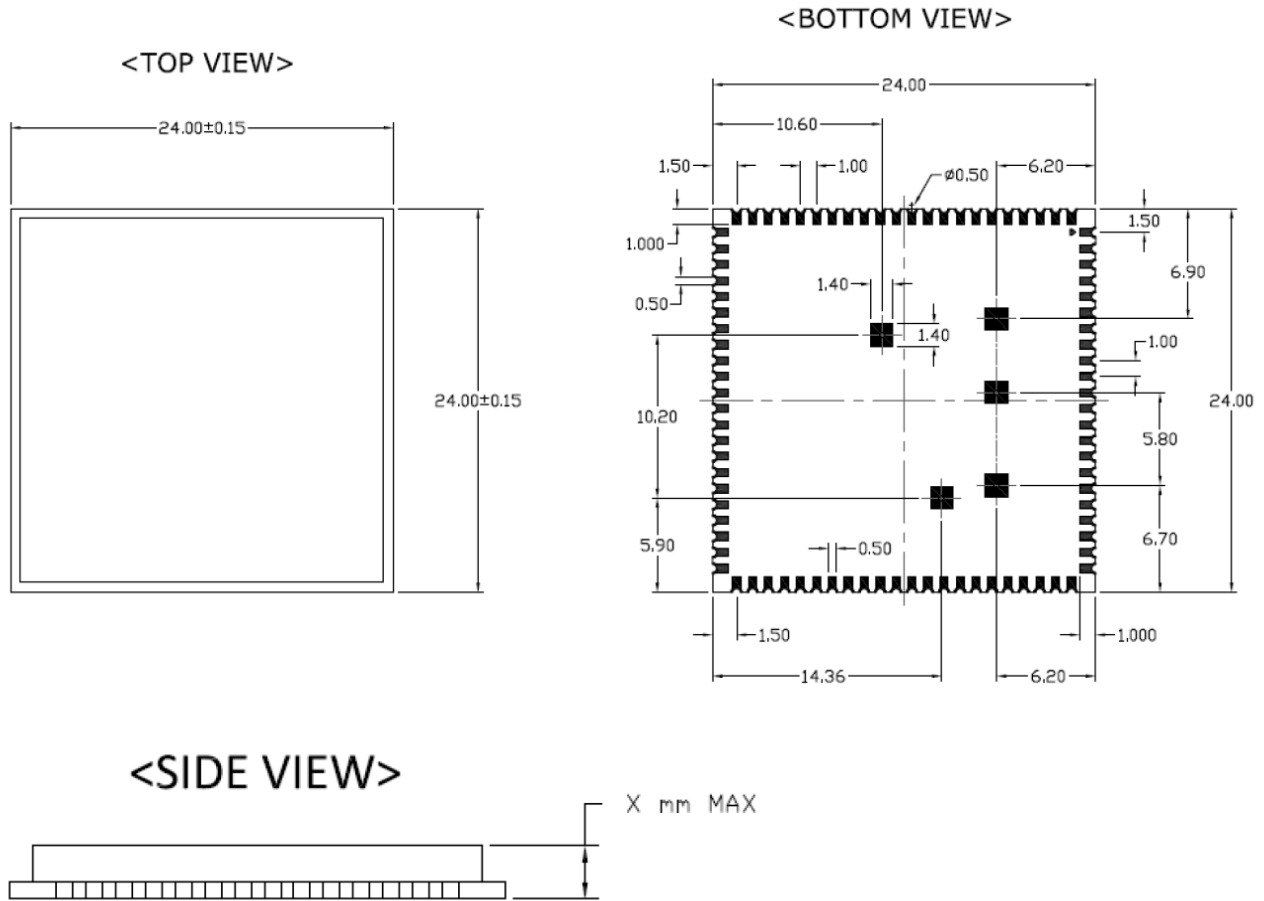
52	LPO_IN	I	External Low Power Clock input (32.768KHz)
53	GND	G	Ground connections
54	VDDIO	P	I/O Voltage supply input
55	GND	G	Ground connections
56	VBAT	P	Main power voltage source input
57	VBAT	P	Main power voltage source input
58	GND	G	Ground connections
59	PCIE_RCLK_N	I	PCI Express differential clock input-Negative
60	PCIE_RCLK_P	I	PCI Express differential clock input-Positive
61	GND	G	Ground connections
62	PCIE_RDP	I	PCI Express receive data-Positive
63	PCIE_RDN	I	PCI Express receive data-Negative
64	GND	G	Ground connections
65	PCIE_TDP	O	PCI Express transmit data-Positive
66	PCIE_TDN	O	PCI Express transmit data-Negative
67	GND	G	Ground connections
68	BT_UART_TXD	O	Bluetooth UART serial data output
69	BT_UART_RXD	I	Bluetooth UART serial data input
70	BT_UART_RTS	O	Bluetooth UART request to send
71	BT_UART_CTS	I	Bluetooth UART clear to send
72	BT_DEV_WAKE	I	HOST wake-up Bluetooth device
73	BT_HOST_WAKE	O	Bluetooth device to wake-up HOST
74	BT_REG_ON	I	Low asserting reset for Bluetooth core
75	GND	G	Ground connections
76	XTAL_IN	I	External Crystal in/ Single clock source in
77	XTAL_OUT	O	External Crystal out
78	GND	G	Ground connections
79	BT_PCM_CLK	I	PCM clock
80	BT_PCM_SYNC	I/O	PCM sync signal
81	BT_PCM_IN	I	PCM data input
81	BT_PCM_IN	I	PCM data input
82	BT_PCM_OUT	O	PCM Data output
83	BT_GPIO2	I/O	BT_GPIO2
84	BT_GPIO3	I/O	BT_GPIO3
85	BT_GPIO4	I/O	BT_GPIO4

86	GND	G	Ground connections
87	BT_ANT	I/O	BT RF port
88	GND	G	Ground connections
EP1	EP1	—	Ground connections
EP2	EP2	—	Ground connections
EP3	EP3	—	Ground connections
EP4	EP4	—	Ground connections
EP5	EP5	—	Ground connections

Note: 1. Each pin has a type, that power (P), ground (G), open-drain (OD), input (I), and output (O).

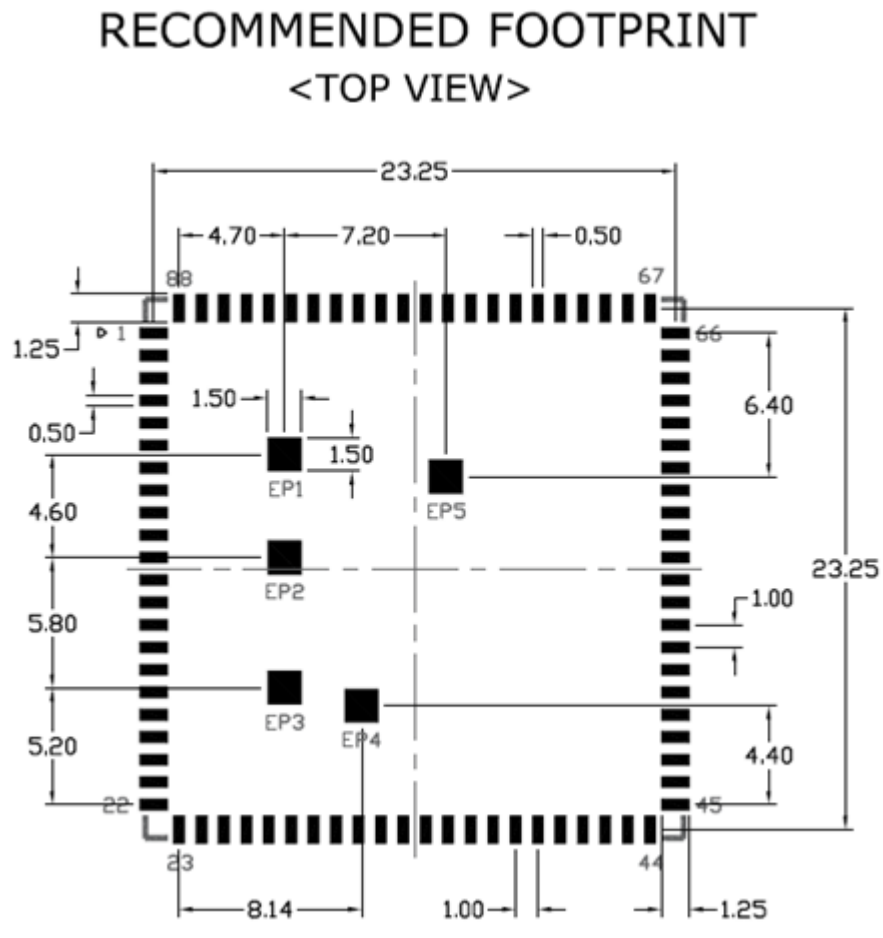
7. Mechanical Specifications

7.1 Module Dimensions

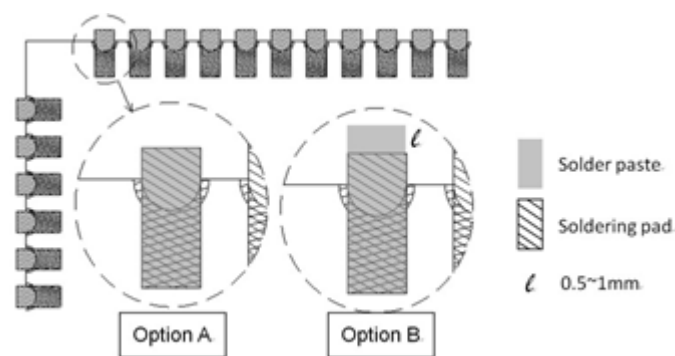


Note, X = 2.1mm

7.2 PCB Footprint



- Solder paste layer design is generally the same as recommended footprint
If soldering quality with good wetting on upright side is essential for PQC, how to optimize the aperture design in the stencil to adjust the amount of solder paste would be crucial. In addition, a kind of stencil design with stepped thickness in partial area would be considered if the thickness of stencil is about 0.1mm or thinner. Please optimize the stencil design by manufacture engineer or contact SparkLAN FAE for assistance.



8. External clock reference

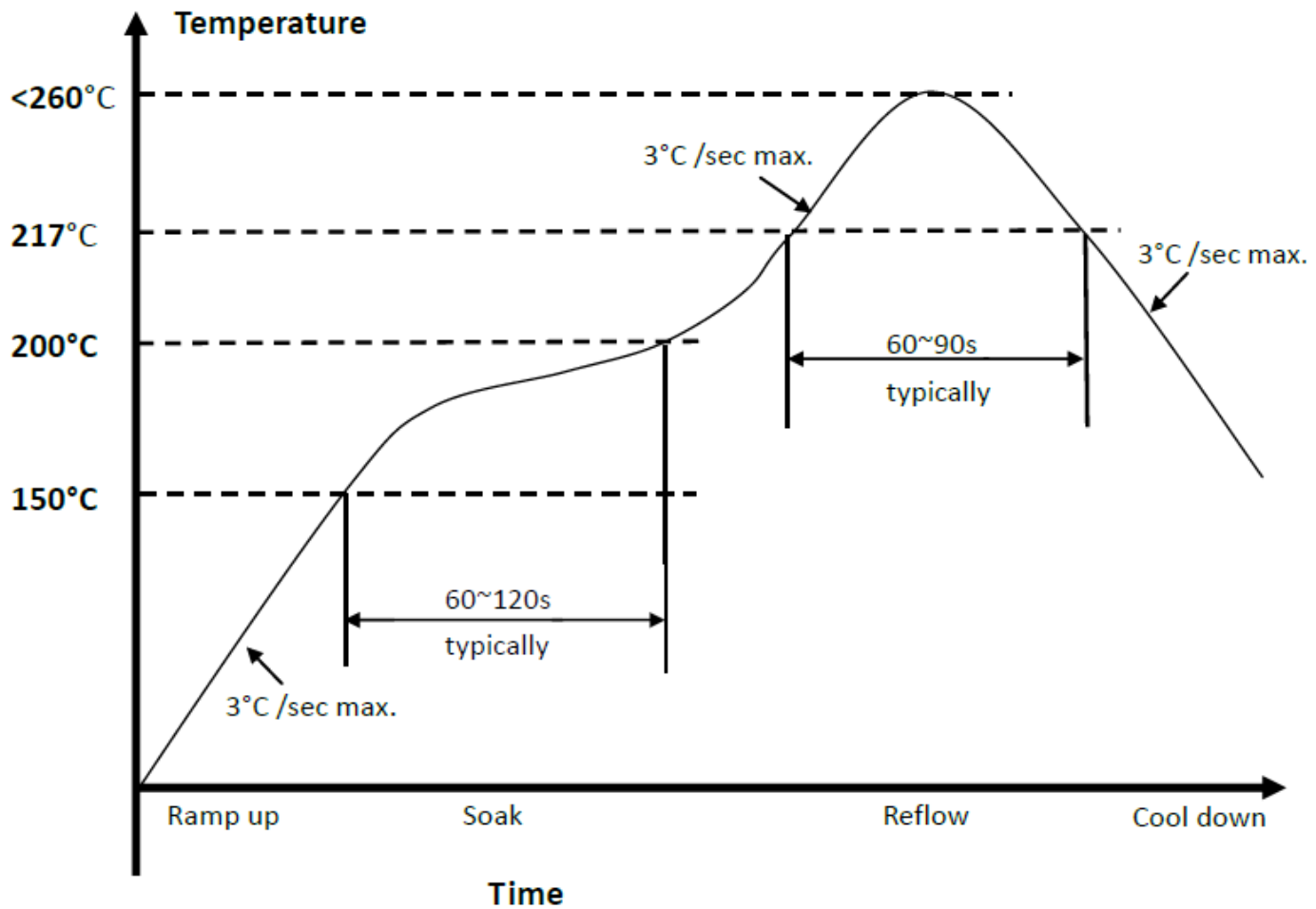
External LPO signal characteristics

Parameter	Specification	Units
Nominal input frequency	32.768	kHz
Frequency accuracy	+/-25	ppm
Duty cycle	30 - 70	%
Input signal amplitude	1.8±0.09	V
Signal type	Square-wave or sine-wave	-
Input impedance	>100k <5	Ω pF
Clock jitter (integrated over 300Hz – 15KHz)	<1	Hz
Output high voltage	0.7V _{io} - V _{io}	V

External 37.4MHz X'TAL characteristics

Parameter	Specification	Units
Nominal input frequency – F0	37.4	MHz
Frequency Tolerance - $\Delta F / F 0$ (At 25°C +/- 3°C)	+/- 10	ppm
Operation Temperature Range - Topr	-30 ~ + 85	°C
Freq. Stability(over operating temperature) - TC Ref. to 25°C	+/- 10	ppm
Load capacitance - CL	18	pF
Equivalent Series Resistance – ESR	Max. 60	Ω
Drive Level - DL	Typ. 50, Max. 100	uW
Insulation resistance – IR At 100Vdc	Min. 500	MΩ

9. Recommended Reflow Profile



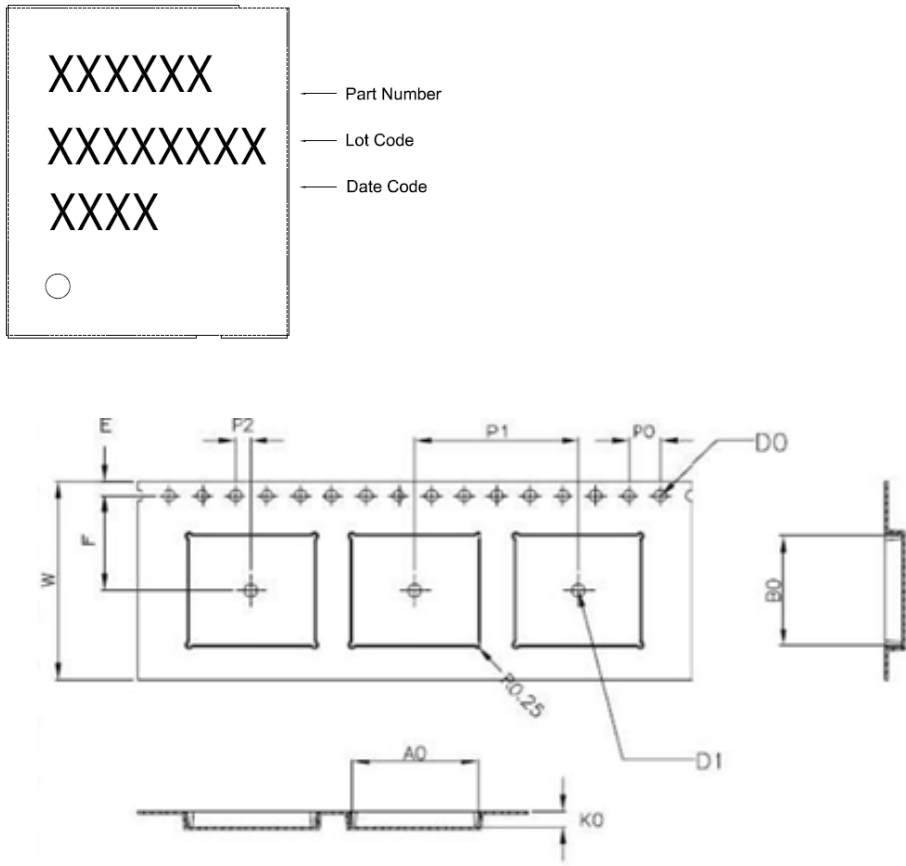
1. Referred to IPC/JEDEC standard
2. Peak Temperature : <260°C
3. Cycle of Reflow: 2 times max.
4. Adding Nitrogen (N₂) to implement 2000ppm or less of oxygen concentration during reflow process is recommended.
5. If the shelf time is exceeded, be sure baking step to remove the moisture from the component

9.1 Caution for SMT Preparation

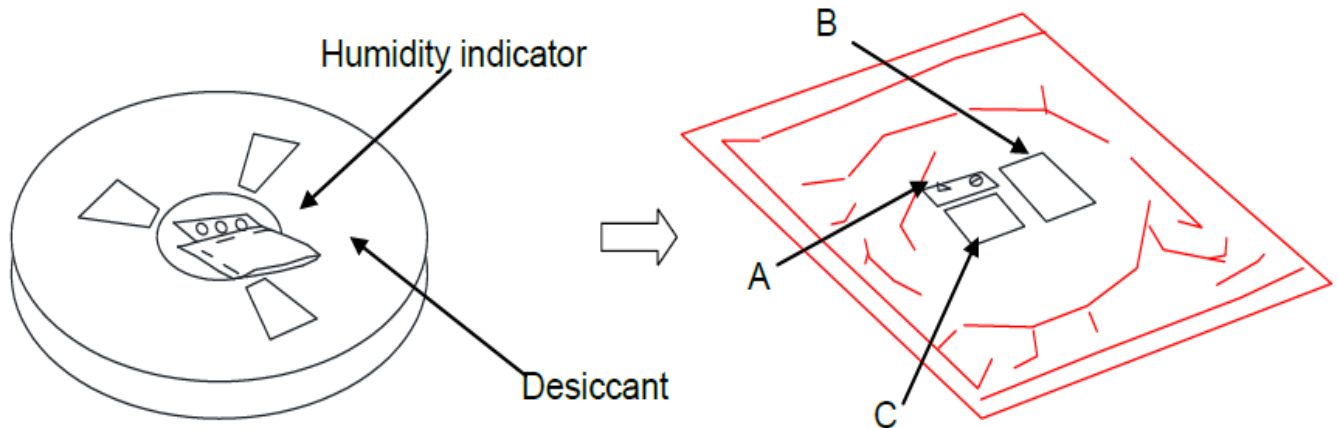
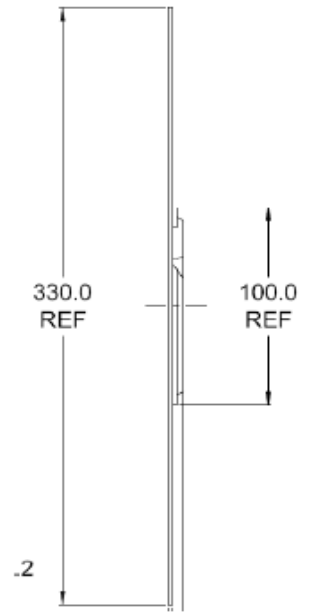
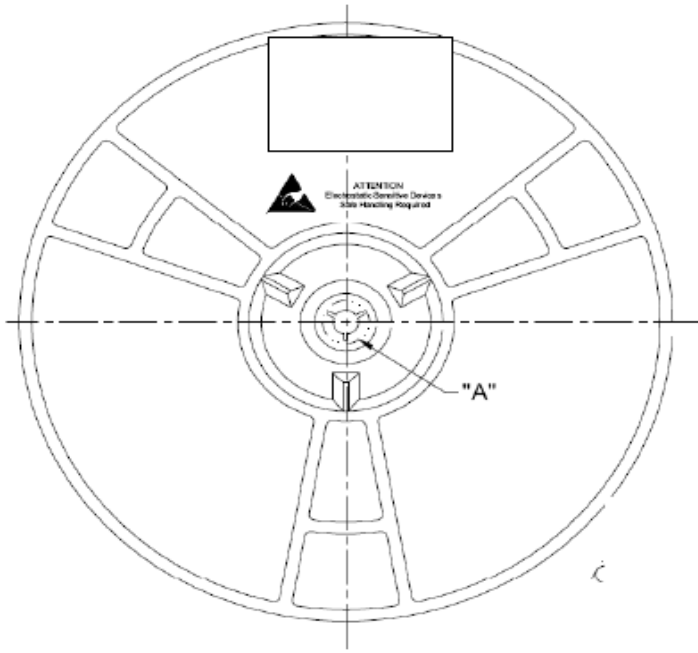
Moisture Sensitivity Level: 4

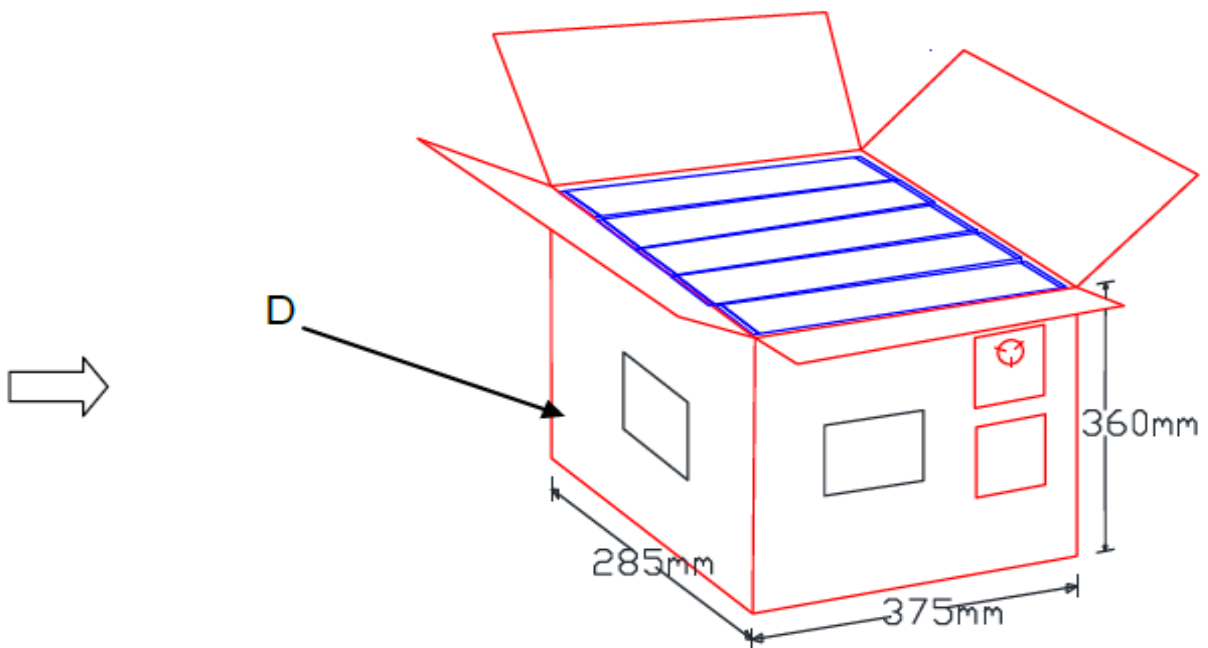
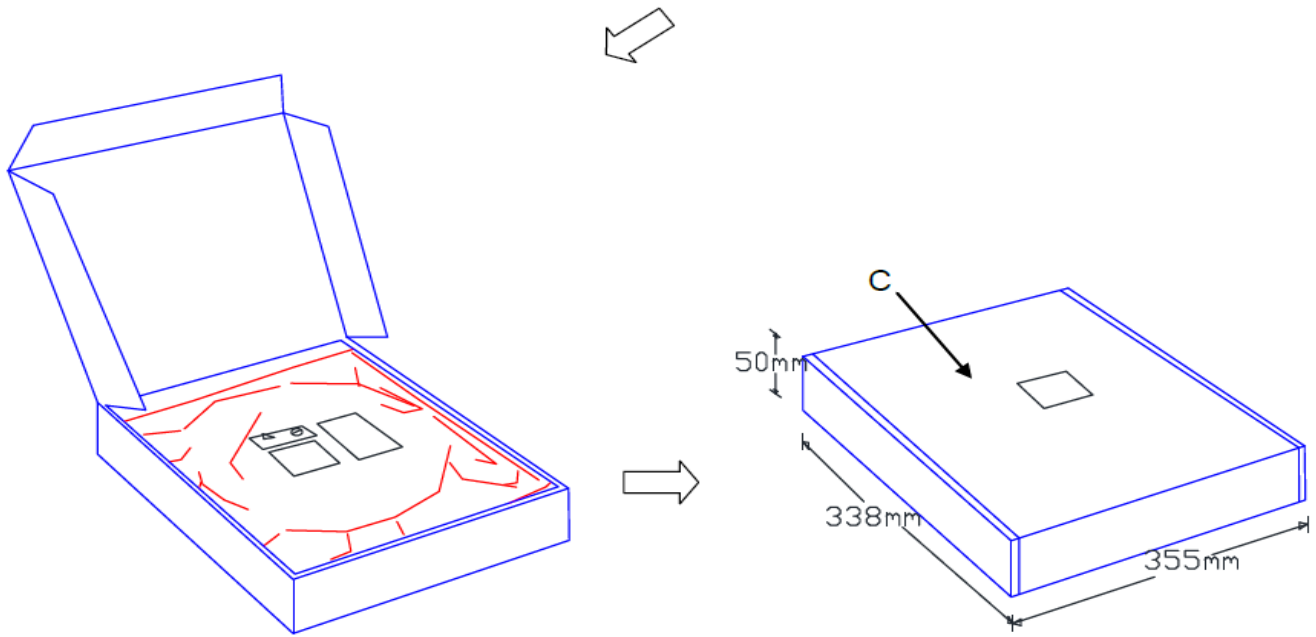
1. Calculated shelf life in sealed bag: 12 months at $<40^{\circ}\text{C}$ and $<90\%$ relative humidity (RH).
2. Peak package body temperature: 250°C .
3. After bag was opened, devices that will be subjected to reflow solder or other high temperature process must be
 - a) Mounted within: 72 hours of factory conditions $\leq 30^{\circ}\text{C}/60\%RH$ or
 - b) Stored per J-STD-033
4. Devices require bake before mounting, if:
 - a) Humidity Indicator Card reads $> 10\%$ for level 2a - 5a devices or $>60\%$ for level 2 devices when read at $23\pm 5^{\circ}\text{C}$
 - b) 3a or 3b are not met.
5. If baking is required, refer to IPC/JEDEC J-STD-033 for bake procedure.

10. Package Information (TBD)



1. 10 sprocket hole pitch cumulative tolerance ± 0.20 .
2. Carrier camber is within 1 mm in 250 mm.
3. Material : Black Conductive Polystyrene Alloy.
4. All dimensions meet EIA-481-D requirements.
5. Thickness: 0.30 ± 0.05 mm.
6. Component load per 13" reel : (TBD) pcs





Note: 1 tape reel = (TBD) box = (TBD) pcs
 1 Carton = (TBD) box = (TBD) pcs

11. Ordering Information

Product Name	Part Number	Description
AP6275HH3	R9701A20003	11ax/ac/a/b/g/n 2T2R WiFi + BT5.0 Combo Sip Module