28.0” 1920 x 360

High brightness color TFT-LCD

Model: VM28B2 V7

Version：01

Date: Oct. 24th, 2023

Note: This specification is subject to change without notice

Customer： _____ **Date：** _____

Approved	**Prepared**
Date:	**Date:**

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RECORD OF REVISION

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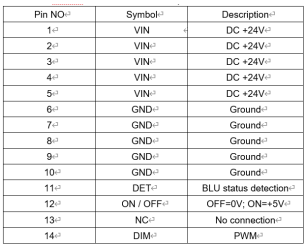
<tr><td>0.3 2023/10/24</td><td>15</td><td> 
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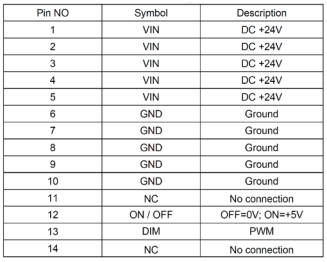
</table></td><td> 
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</table></td><td></td></tr>
</table>

1. Handling Precautions

1) Since front polarizer is easily damaged, pay attention not to scratch it.
2) Be sure to turn off power supply when inserting or disconnecting from input connector.
3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
7) Do not open or modify the Module Assembly.
8) Do not press the reflector sheet at the back of the module to any directions.
9) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
10) After installation of the TFT Module into an enclosure, do not twist nor bend the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.

2. General Description

2.1 Overview

This specification applies to the Color Active Matrix Liquid Crystal Display composed of a TFT-LCD display a LED backlight system. The screen format is intended to support (1920(H) x 360(V) screen and 16.7M colors.
LED driving board for backlight unit is included.

2.2 Features

- High brightness display, 2500nits by LED backlight.
- 100K Hrs backlight life
- Wide view angle
- RoHS Compliance

2.3 Application

Industrial applications.

2.4 Display specifications

Items	Unit	Specification
Screen Diagonal	mm	28.0inch
Active Area	mm	698.4 (H) X 130.95(V)
Pixels H x V	pixels	1920 x3(RGB) x 360
Pixels Pitch	um	363.7 (per one triad) x 363.7
Pixel Arrangement		RGB Vertical stripe
Display mode		Normally Black
White luminance (center)	Cd/m^2	2500 (Typ)
Contrast ratio		4000 : 1
Optical Response Time	msec	8 ms (Typ. On/off)
Normal Input Voltage VDD	Volt	12.0
Power Consumption (Vcc Line + LED backlight)	Watt	47.1W (VDD line=5.1 W; LED lines= 42W)
Weight	Grams	TBD
Physical size	mm	722.2 (W)×154.75 (H)×28.9 (D)
Electrical Interface		LVDS
Support colors		16.7M colors
Surface Treatment		Anti-glare and hard-coating 3H
Temperature range Operating Storage	 ^0C ^0C	 -20 ~ 60 -20 ~ 60
RoHS Compliance		RoHS Compliance

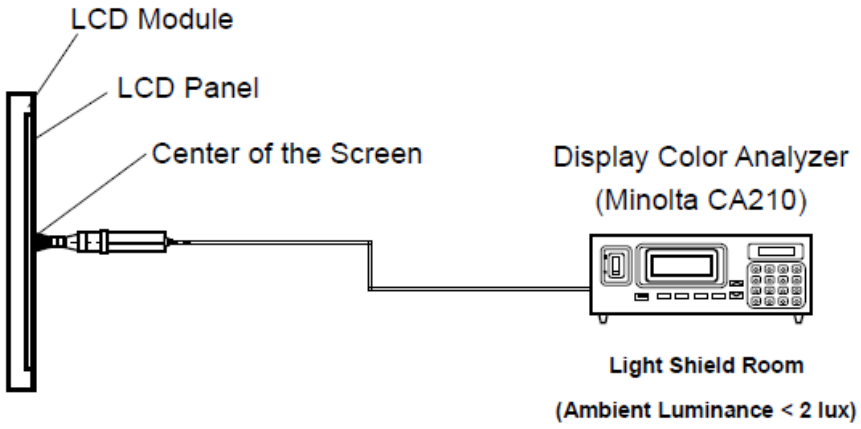
2.5 Optical characteristics

The following optical characteristics are measured under stable condition at 25 ^{0}C

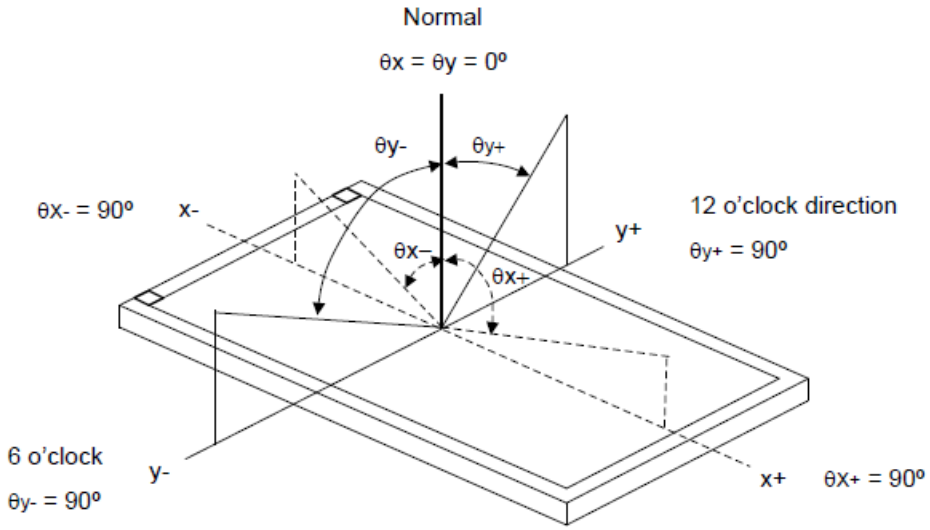
Items	Unit	Conditions	Min.	Typ.	Max.	Note
Viewing angle	Deg.	Horizontal (Right)	85	89		2
		CR=10 (Left)	85	89		
		Vertical (Up)	85	89		
		CR=10 (Down)	85	89		
Contrast Ratio		Normal Direction	3200	4000		3
Response Time	msec	Raising + Falling		8	10	4
Color / Chromaticity Coordinates (CIE)		Red x	-0.05	0.653	+0.05	5
		Red y		0.336		
		Green x		0.323		
		Green y		0.615		
		Blue x		0.152		
		Blue y		0.067		
Color coordinates (CIE) White		White x		0.313		
		White y		0.329		
Center Luminance	Cd/m^2		2000	2500		6
Luminance Uniformity	%		70	75		7
NTSC	%			72		
Crosstalk (in 60 Hz)	%				1.5	
Flicker	dB				-20	

Note 1: Measurement method

The LCD module should be stabilized at given temperature for 0.5 hour to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 1 hour in a windless room.



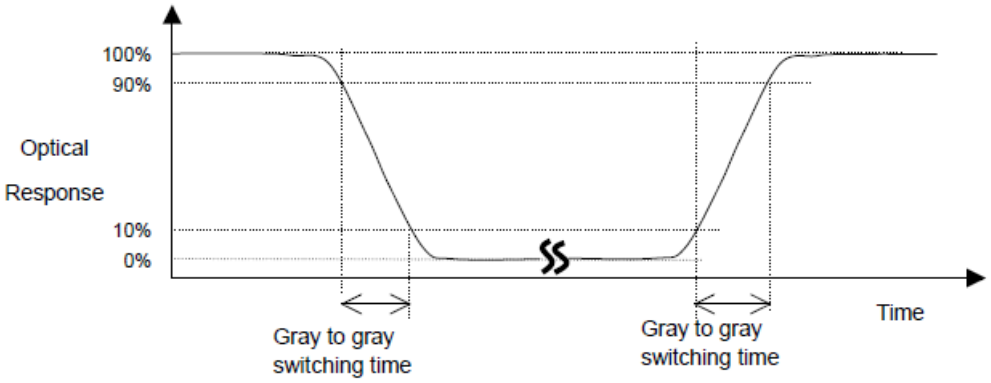
Note 2: Definition of viewing angle



Note 3: Contrast ratio is measured by Minolta CA210

Note 4: Definition of Response time

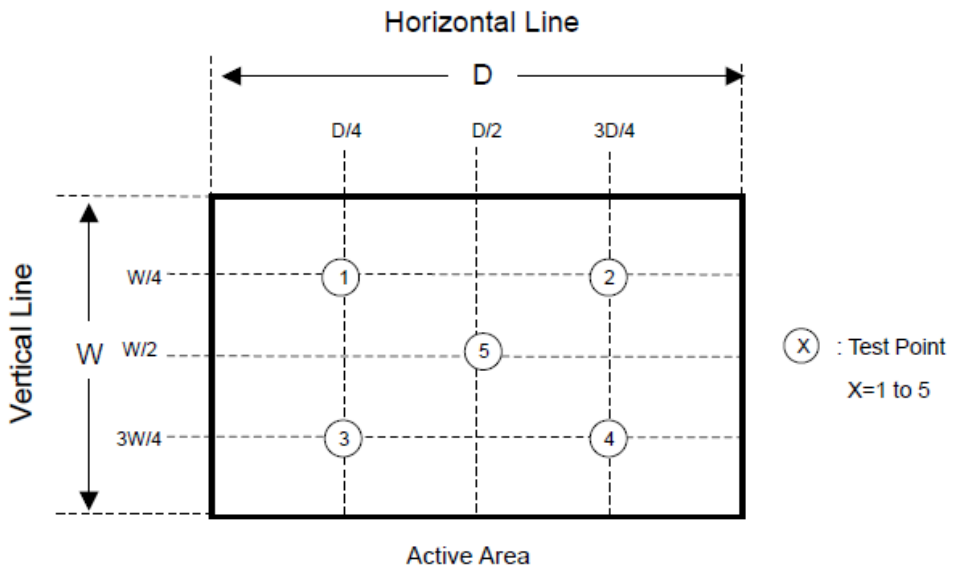
The output signals of photo detector are measured when the input signals are changed from “Full Black” to “Full White” (rising time), and from “Full White” to “Full Black” (falling time), respectively. The response time is interval between the 10% and 90% of amplitudes. Please refer to the figure as below.



Note 5: Color chromaticity and coordinates (CIE) is measured by Minolta CA210

Note 6: Center luminance is measured by Minolta CA210

Note 7: Luminance uniformity of these 5 points is defined as below and measured by Minolta CA210



Uniformity = (Min. Luminance of 5 points) / (Max. Luminance of 5 points)

3. Absolute Maximum Ratings

Absolute maximum ratings of the module are as following:

3.1 TFT LCD module

Items	Symbol	Min	Max	Unit	Conditions
Logic supply voltage	V_{DD}	-0.3	14	Volt	Note 1, 2

3.2 Backlight unit

Items	Symbol	Min	Max	Unit	Conditions
BLU input voltage			25.2	V	

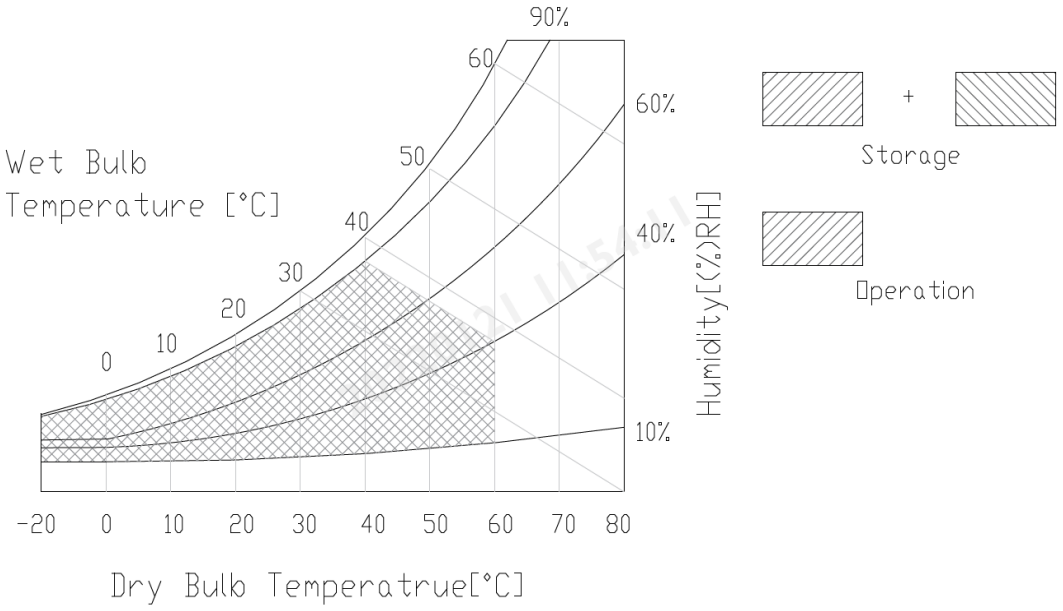
3.3 Environment

Items	Symbol	Values			Unit	Conditions
		Min.	Typ.	Max.		
Operation temperature	T_{OP}	-20	-	60	^{0}C	Note 3
Operation Humidity	H_{OP}	10		85	%	
Storage temperature	T_{ST}	-20		60	^{0}C	
Storage Humidity	H_{ST}	5		90	%	

Note 1: With in Ta= 25℃

Note 2: Permanent damage to the device may occur if exceed maximum values

Note 3: For quality performance, please refer to IIS (Incoming Inspection Standard).



4. Interface specification

4.1 Input power

This module requires power inputs which are employed to power the LCD electronics and to drive the TFT array and liquid crystal.

Item		Symbol	Min.	Typ.	Max	Unit	Note
Power Supply Input Voltage		V_{DD}	10.8	12	13.2	V	1
Power Supply Input Current	Black pattern	I_{DD}	--	0.3	0.36	A	2
	White pattern		--	0.42	0.51	A	
Power Consumption	Black pattern	P_C	--	3.6	4.3	Watt	
	White pattern		--	5.1	6.2	Watt	
Inrush Current		I_{RUSH}	--	--	3	A	3

Note1. The ripple voltage should be fewer than 5% of VDD.

Note2. Test Condition:

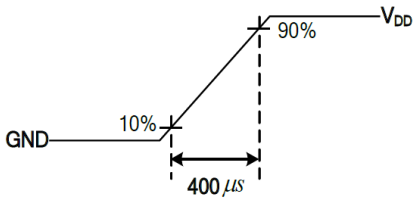
(1) V_{DD} = 12.0V, (2) Fv = 60Hz, (3) Fclk= 74.25MHz, (4) Temperature = 25 ℃

(5) Power dissipation check pattern. (Only for power design)

a. Black pattern

b. White pattern

Note3. Measurement condition : Rising time = 400us



4.2 Backlight unit

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks (Test Condition)
Input Specification						
Input Voltage	**V_{in}**	22.8	24	25.2	V_{DC}	Input voltage: 24 V_{DC}
Input Current	**I_{in}**		1.75		A_{DC}	
BLU power	**P_{BLU}**		42		W	
On/Off control	**ON/OFF**	3.3	-	5.5	V_{DC}	ON STATE
		-	0	0.8		OFF STATE
Dimming (PWM)	**DIM**	2	-	5.5	V_{DC}	High level
		0	-	0.8		Low level
		10		100	%	Dimming range
		200	300	500	Hz	Dimming frequency
BLU lifetime	**MTBF**		100,000		hr	

4.3 Interface connector

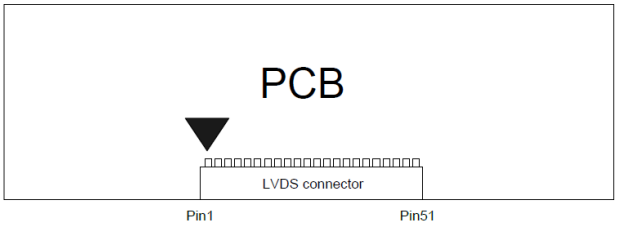
4.3.1 TFT connector(CN1)

■ LCD connector: FI-RTE51SZ-HF (JAE, LVDS connector) or compatible(CHIEF LAND 115E51-0000RA - M3-R / P-two 187059-5122)

PIN	Symbol	Description	Note
1	N.C.	No connection(for AUO test only. Do not connect)	2
2	N.C.	No connection(for AUO test only. Do not connect)	2
3	N.C.	No connection(for AUO test only. Do not connect)	2
4	N.C.	No connection(for AUO test only. Do not connect)	2
5	N.C.	No connection(for AUO test only. Do not connect)	2
6	N.C.	No connection(for AUO test only. Do not connect)	2
7	LVDS_SEL	Open/High(3.3V) for NS, Low(GND) for JEIDA	3
8	N.C.	No connection(for AUO test only. Do not connect)	2
9	N.C.	No connection(for AUO test only. Do not connect)	2
10	N.C.	No connection(for AUO test only. Do not connect)	2
11	GND	Ground	
12	CH1_Y0-	LVDS Channel 1, Signal 0-	
13	CH1_Y0+	LVDS Channel 1, Signal 0+	
14	CH1_Y1-	LVDS Channel 1, Signal 1-	
15	CH1_Y1+	LVDS Channel 1, Signal 1+	
16	CH1_Y2-	LVDS Channel 1, Signal 2-	
17	CH1_Y2+	LVDS Channel 1, Signal 2+	
18	GND	Ground	
19	CH1_CLK-	LVDS Channel 1, Clock -	
20	CH1_CLK+	LVDS Channel 1, Clock +	
21	GND	Ground	
22	CH1_Y3-	LVDS Channel 1, Signal 3-	
23	CH1_Y3+	LVDS Channel 1, Signal 3+	
24	N.C.	No connection	2
25	N.C.	No connection	2
26	N.C.	No connection(for AUO test only. Do not connect)	
27	N.C.	No connection(for AUO test only. Do not connect)	
28	CH2_Y0-	LVDS Channel 2, Signal 0-	
29	CH2_Y0+	LVDS Channel 2, Signal 0+	
30	CH2_Y1-	LVDS Channel 2, Signal 1-	
31	CH2_Y1+	LVDS Channel 2, Signal 1+	
32	CH2_Y2-	LVDS Channel 2, Signal 2-	
33	CH2_Y2+	LVDS Channel 2, Signal 2+	

34	GND	Ground	
35	CH2_CLK-	LVDS Channel 2, Clock -	
36	CH2_CLK+	LVDS Channel 2, Clock +	
37	GND	Ground	
38	CH2_Y3-	LVDS Channel 2, Signal 3-	
39	CH2_Y3+	LVDS Channel 2, Signal 3+	
40	N.C.	No connection(for AUO test only. Do not connect)	2
41	N.C.	No connection(for AUO test only. Do not connect)	2
42	N.C.	No connection(for AUO test only. Do not connect)	2
43	N.C.	No connection(for AUO test only. Do not connect)	2
44	GND	Ground	
45	GND	Ground	
46	GND	Ground	
47	N.C.	No connection(for AUO test only. Do not connect)	2
48	V_{DD}	Power Supply, +12V DC Regulated	
49	V_{DD}	Power Supply, +12V DC Regulated	
50	V_{DD}	Power Supply, +12V DC Regulated	
51	V_{DD}	Power Supply, +12V DC Regulated	

Note1. Pin number start from the left side as the following figure.

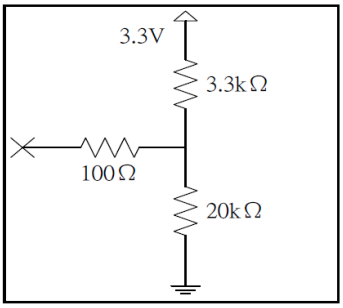


Note2. Please leave this pin unoccupied. It cannot be connected with any signal (Low/GND/High).

Note3. LVDS data format selection

LVDS_SEL	Mode
H or OPEN	NS
L	Jeida

Input equivalent impedance of LVDE_SEL pin



4.3.2 Backlight connector

4.3.2.1 Master (CN2)

Connector: CviLux CI0114M1HR0 or equivalent

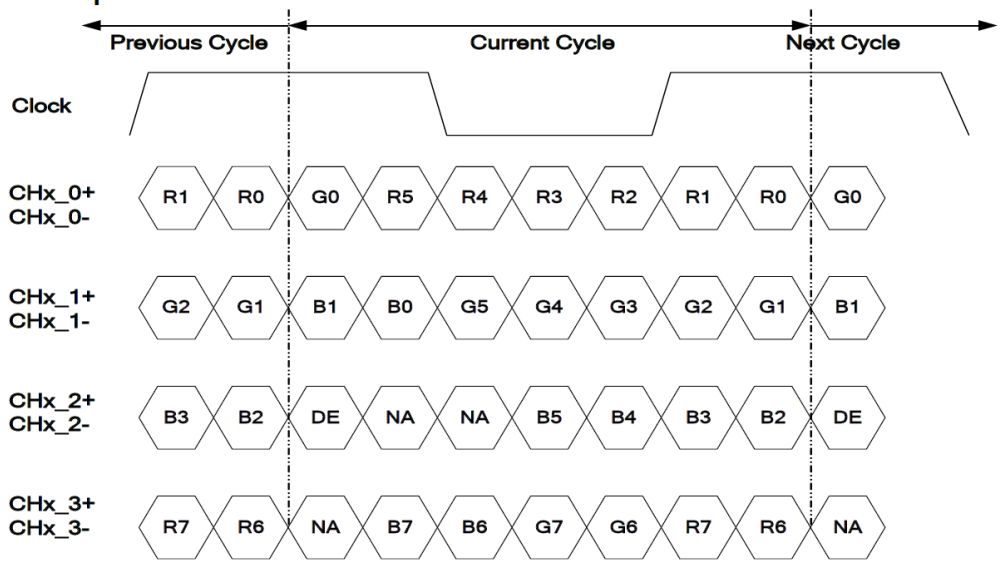
Pin NO	Symbol	Description
1	VIN	DC +24V
2	VIN	DC +24V
3	VIN	DC +24V
4	VIN	DC +24V
5	VIN	DC +24V
6	GND	Ground
7	GND	Ground
8	GND	Ground
9	GND	Ground
10	GND	Ground
11	NC	No connection
12	ON / OFF	OFF=0V; ON=+5V
13	DIM	PWM
14	NC	No connection

4.4 Input data format

4.4.1 LVDS color data mapping

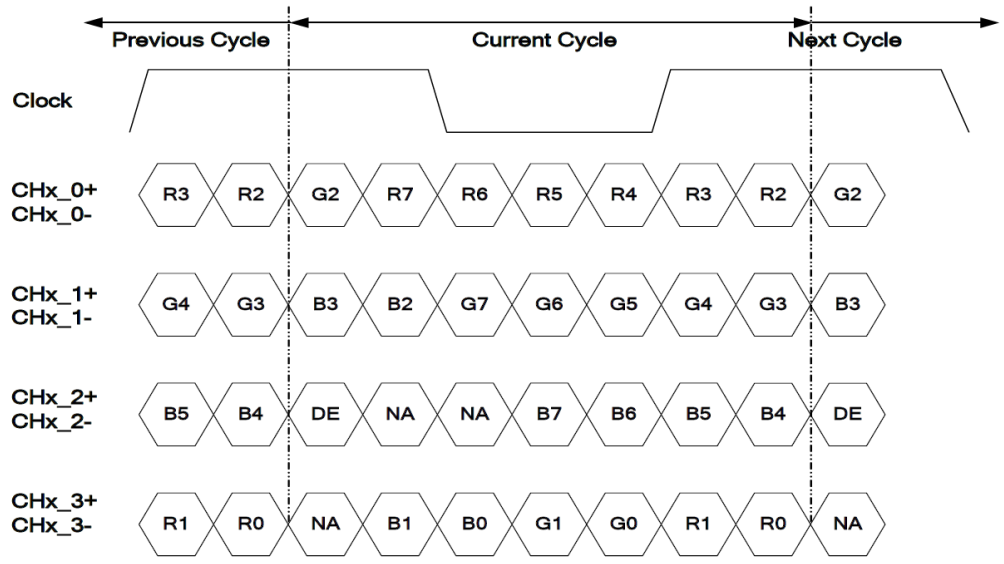
LVDS Option for 8bit

■ **LVDS Option NS**



Note: x = 1, 2, 3, 4…

■ **LVDS Option JEIDA**



Note: x = 1, 2, 3, 4…

4.4.2 Color input data reference

The brightness of each primary color (red, green and blue) is based on the 8 bit gray scale data input for the color; the higher the binary input, the brighter the color. The table below provides a reference for color versus data input.

COLOR DATA REFERENCE

8bit

Color		Input Color Data																							
		RED								GREEN								BLUE							
		MSB							LSB	MSB							LSB	MSB							LSB
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
Basic Color	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Blue(255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R	RED(000)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED(001)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	RED(254)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED(255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
G	GREEN(000)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	GREEN(001)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

	GREEN(254)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	GREEN(255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
B	BLUE(000)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	BLUE(001)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

	BLUE(254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	BLUE(255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

5. Signal timing specification

5.1 Input timing

5.1.1 Timing table

Timing Table (DE only Mode)

Signal	Item	Symbol	MIN	TYP	MAX	Unit
Vertical Section	Period	Tv	1120	1125	1480	Th
	Active	Tdisp(v)		1080		Th
	Blanking	Tblk(v)	40	45	400	Th
Horizontal Section	Period	Th	1030	1100	1325	Tclk
	Active	Tdisp(h)		960		Tclk
	Blanking	Tblk(h)	70	140	365	Tclk
Vertical Frequency	Frequency	Freq	47	60	63	Hz
Horizontal Frequency	Frequency	Freq	60	67.5	73	KHz
Clock	Frequency	FCLK	53	74.25	82	MHz

Notes:

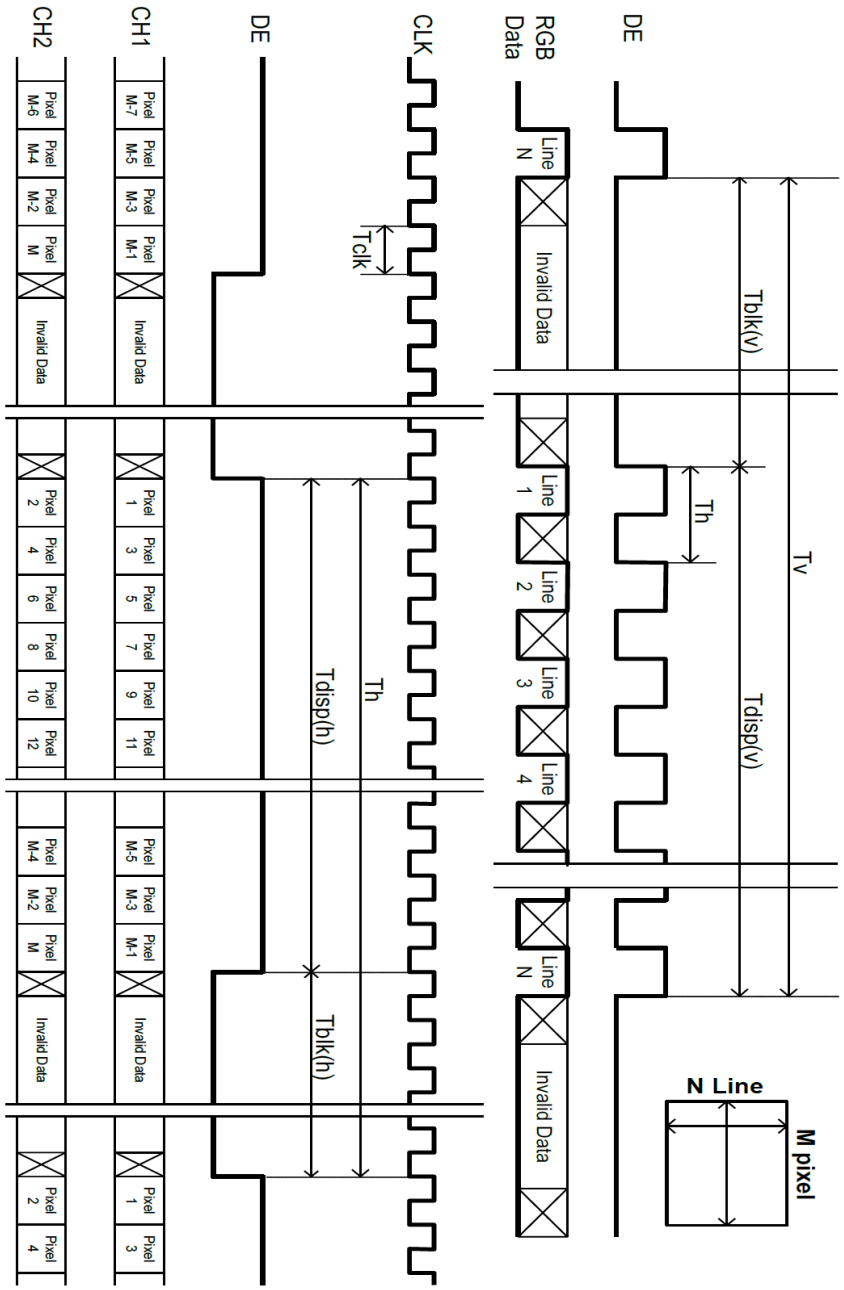
(1) Display position is specific by the rise of DE signal only.
Horizontal display position is specified by the rising edge of 1st DCLK after the rise of 1st DE, is displayed on the left edge of the screen.

(2) Vertical display position is specified by the rise of DE after a “Low” level period equivalent to eight times of horizontal period. The 1st data corresponding to one horizontal line after the rise of 1st DE is displayed at the top line of screen.

(3) If a period of DE “High” is less than 3840 DCLK or less than 2160 lines, the rest of the screen displays black.

(4) The display position does not fit to the screen if a period of DE “High” and the effective data period do not synchronize with each other.

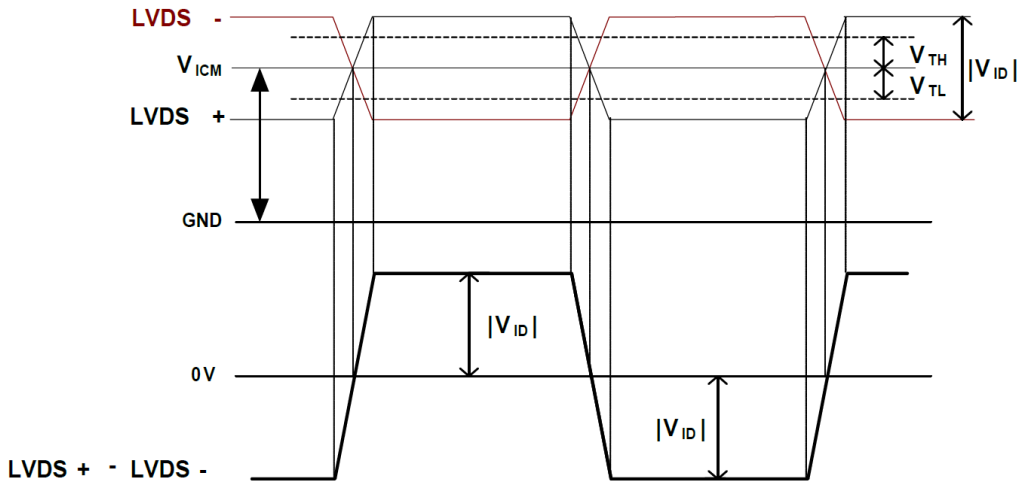
5.1.2 Signal timing waveform



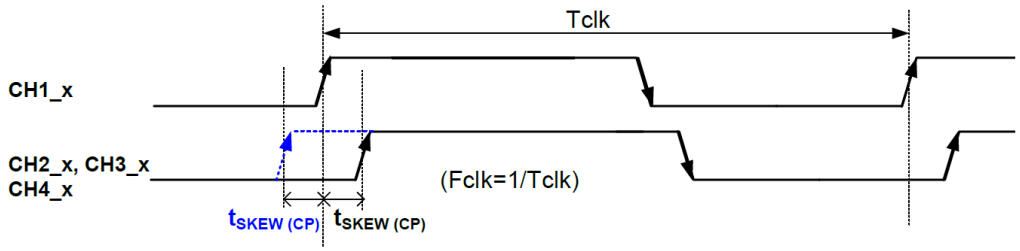
5.2 Input interface characteristics

Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max		
LVDS Interface	Input Differential Voltage	$\lvert V_{ID} \rvert$	200	400	600	mV_{DC}	1
	Differential Input High Threshold Voltage	V_{TH}	+100	--	+300	mV_{DC}	1
	Differential Input Low Threshold Voltage	V_{TL}	-300	--	-100	mV_{DC}	1
	Input Common Mode Voltage	V_{ICM}	1.1	1.25	1.4	V_{DC}	1
	Input Channel Pair Skew Margin	$t_{SKEW\ (CP)}$	-500	--	+500	ps	2
	Input Channel Pair Skew Margin (only for M'Star MST7428BB)	$t_{SKEW\ (CP)}$	-400	--	+400	ps	2
	Receiver Clock : Spread Spectrum Modulation range	Fclk_ss	Fclk -3%	--	Fclk +3%	MHz	3
	Receiver Clock : Spread Spectrum Modulation frequency	Fss	30	--	200	KHz	3
	Receiver Data Input Margin Fclk = 85 MHz Fclk = 65 MHz	tRMG	 -0.4 -0.5	 -- --	 0.4 0.5	ns	8

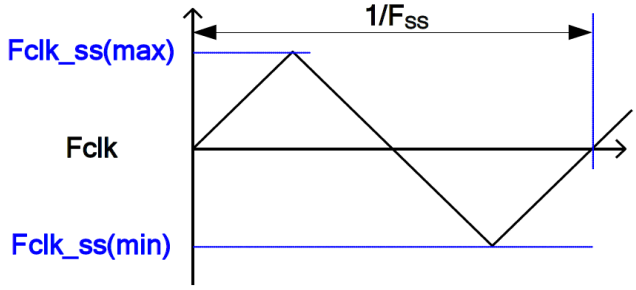
Note1. VICM = 1.25V



Note2. Input Channel Pair Skew Margin

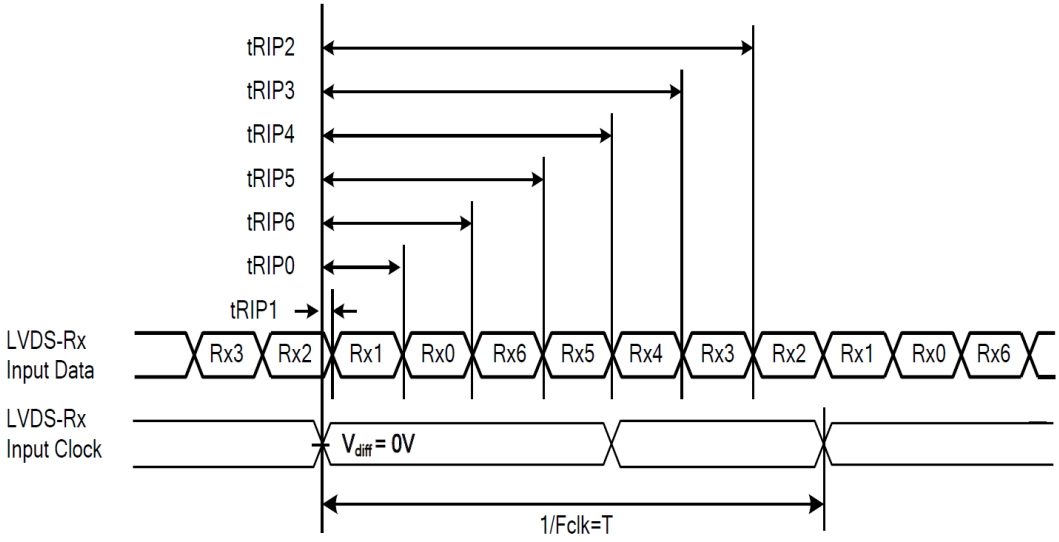


Note3. LVDS Receiver Clock SSCG (Spread spectrum clock generator) is defined as below figures.

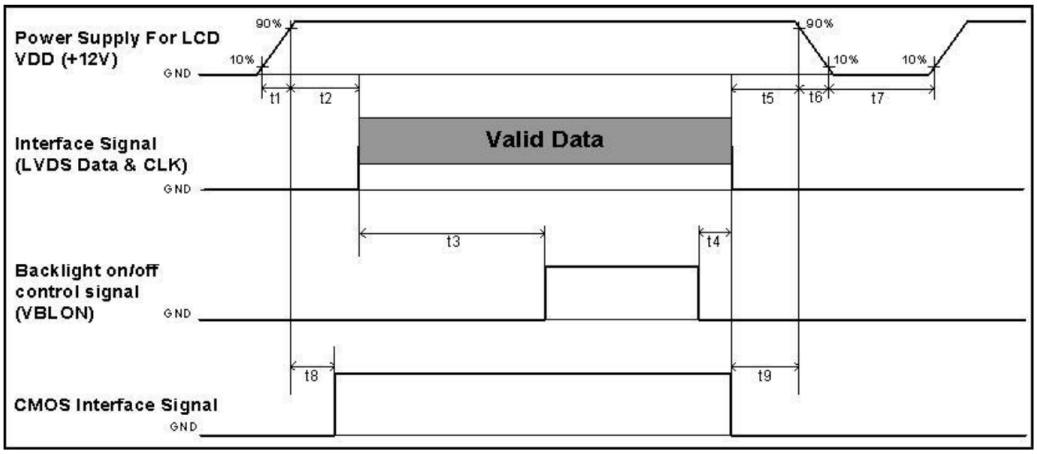


Note4. Receiver Data Input Margin

Parameter	Symbol	Rating			Unit	Note
		Min	Type	Max		
Input Clock Frequency	Fclk	Fclk (min)	--	Fclk (max)	MHz	**T=1/Fclk**
Input Data Position0	tRIP1	-|tRMG|	0	|tRMG|	ns	
Input Data Position1	tRIP0	T/7-|tRMG|	T/7	T/7+|tRMG|	ns	
Input Data Position2	tRIP6	2T/7-|tRMG|	2T/7	2T/7+|tRMG|	ns	
Input Data Position3	tRIP5	3T/7-|tRMG|	3T/7	3T/7+|tRMG|	ns	
Input Data Position4	tRIP4	4T/7-|tRMG|	4T/7	4T/7+|tRMG|	ns	
Input Data Position5	tRIP3	5T/7-|tRMG|	5T/7	5T/7+|tRMG|	ns	
Input Data Position6	tRIP2	6T/7-|tRMG|	6T/7	6T/7+|tRMG|	ns	



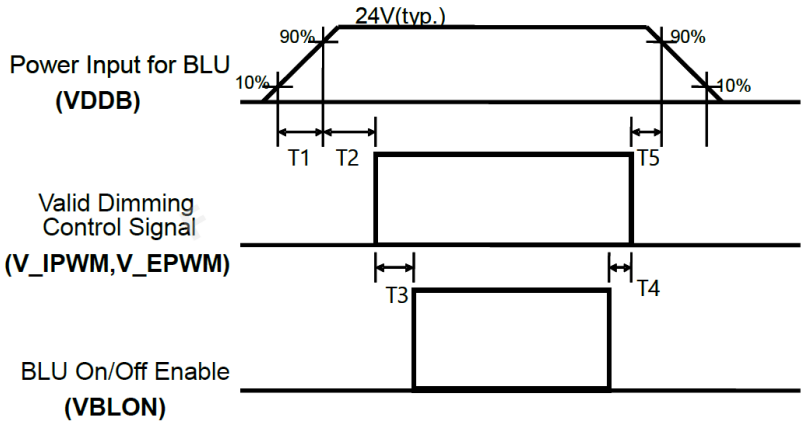
5.3 Power sequence for LCD



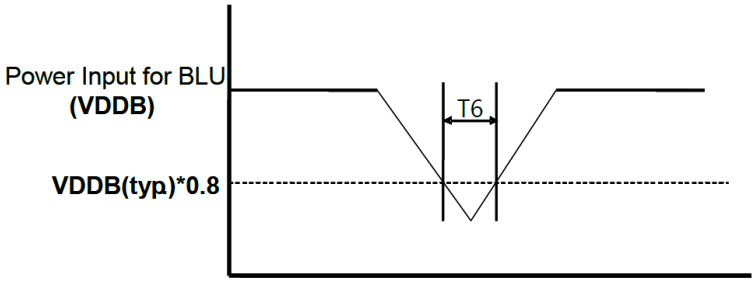
Parameter	Values			Unit
	Min.	Type.	Max.	
t1	0.4	---	30	ms
t2	40	---	---	ms
t3	640	---	---	ms
t4	0*1	---	---	ms
t5	0	---	---	ms
t6	---	---	---*2	ms
t7	1000	---	---	ms
t8	20*3	---	50	ms
t9	0	---	---	ms

Note:
(1) t4=0 : concern for residual pattern before BLU turn off.
(2) t6 : voltage of VDD must decay smoothly after power-off. (customer system decide this value)
(3) When user control signal is N.C. (no connection), opened in Transmitted end, t8 timing spec can be negligible.

5.4 Power sequence for BLU



Dip condition



Parameter	Min	Typ	Max	Units
T1	20	-	-	ms *1
T2	250	-	-	ms
T3	2200			ms
T4	0	-	-	ms
T5	0	-	-	ms
T6		-	1000	ms*2

Note:1. T6 describes VDDB dip condition and VDDB couldn't lower than 10% VDDB.

6. Reliability Test

Environment test conditions are listed as following table.

Items	Required Condition	Note
Temperature Humidity Bias (THB)	Ta=40℃, 80%RH, 120hours	
High Temperature Operation (HTO)	Ta= 60℃, 120hours	3
Low Temperature Operation (LTO)	Ta= -20℃, 120hours	
High Temperature Storage (HTS)	Ta= 60℃, 120hours	
Low Temperature Storage (LTS)	Ta= -20℃, 120hours	
Thermal Shock Test (TST)	-20℃/30min, 60℃/30min, 100 cycles	
On/Off Test	On/10sec, Off/10sec, 30,000 cycles	
ESD (ElectroStatic Discharge)	Contact Discharge: ± 8KV, 150pF(330Ω) 1sec/cycle.	
	Air Discharge: ± 15KV, 150pF(330Ω) 1sec/cycle	

Note 1: The TFT-LCD module will not sustain damage after being subjected to 100 cycles of rapid temperature change. A cycle of rapid temperature change consists of varying the temperature from -10℃ to 50℃, and back again. Power is not applied during the test. After temperature cycling, the unit is placed in normal room ambient for at least 4 hours before power on.

Note 2: According to EN61000-4-2 , ESD class B: Some performance degradation allowed. No data lost. Self-recoverable. No hardware failures.

Note 3: TFT surface

Note 4: There should be no condensation on the surface of panel during test.

Note 5: In the standard conditions, there is no function failure issue occurred. All the cosmetic specification is judged before reliability test.

Note 6: Before cosmetic and function test, the product must have enough recovery time, at least 4 hours at room temperature.

7. Shipping package
(TBD)

8. Mechanical Characteristics