37.0” Stretched
High brightness color TFT-LCD Module

Model: VM37B1 V2

Date: Apr. 8th, 2020

Note: This specification is subject to change without notice

Customer： _____ **Date：** _____

Approved	**Prepared**
Date:	**Date:**

Contents

RECORD OF REVISION

Version and Date	Page	Old description	New description	Remark
0.1 2020/04/08	All	First Edition for customer		

1. Handling Precautions

1) Since front polarizer is easily damaged, pay attention not to scratch it.
2) Be sure to turn off power supply when inserting or disconnecting from input connector.
3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
7) Do not open or modify the Module Assembly.
8) Do not press the reflector sheet at the back of the module to any directions.
9) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
10) After installation of the TFT Module into an enclosure, do not twist nor bend the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.

2. General Description

2.1 Overview

This specification applies to the Color Active Matrix Liquid Crystal Display composed of a TFT-LCD display a LED backlight system. The screen format is intended to support (1920(H) x 540(V)) screen and 1.07B colors.
LED driving board for backlight unit included.

2.2 Features

- High brightness display, 1300nits by LED backlight.
- Long operation lifetime BLU design
- RoHS Compliance
- Extreme wide temperature LC(-40~110℃) applied

2.3 Application

Industrial applications.

2.4 Display specifications

Items	Unit	Specification
Screen Diagonal	mm	37.0 inch
Active Area	mm	904.32(H) X 254.34(V)
Pixels H x V	pixels	1920 x3(RGB) x 540
Pixels Pitch	um	470 (per one triad) x 470
Pixel Arrangement		RGB Vertical stripe
Display mode		Normally Black
White luminance (center)	Cd/m^2	1300 (Typ)
Contrast ratio		4000:1 (Typ.)
Optical Response Time	msec	8 ms (Typ. On/off)
Normal Input Voltage VDD	Volt	12V
Power Consumption (Vcc Line + LED backlight)	Watt	59.26W (VDD line=5.76 W; LED lines= 53.5 W)
Weight	Grams	TBD
Physical size	mm	923.3 (W)×277.1(H)×30.05D)
Electrical Interface		LVDS
Support colors		1.07B colors
Surface Treatment		Anti-glare and hard-coating 3H
Temperature range Operating Storage	 ^0C ^0C	 0 ~ 50 -20 ~ 60
RoHS Compliance		RoHS Compliance

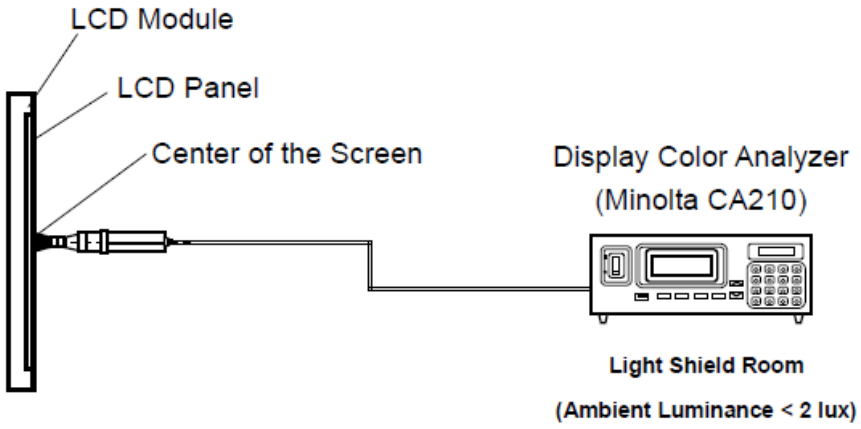
2.5 Optical characteristics

The following optical characteristics are measured under stable condition at 25 ^{0}C

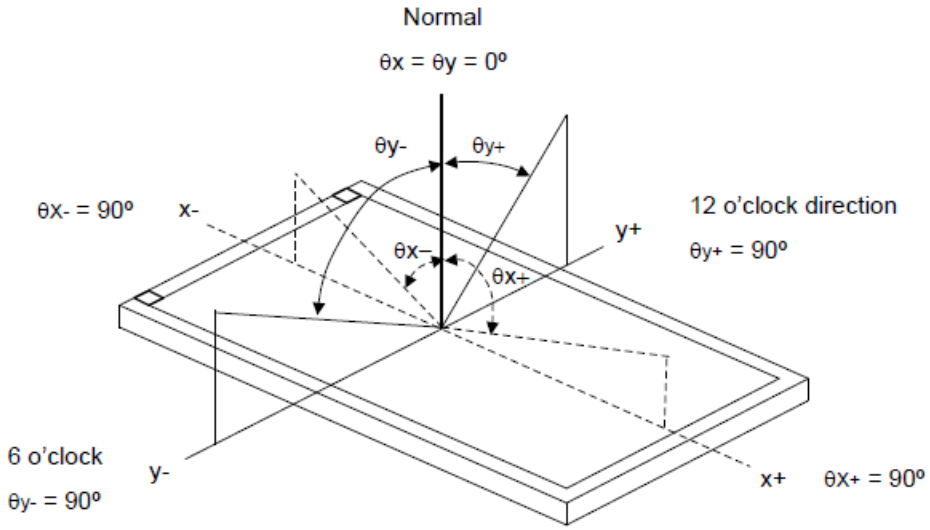
Items	Unit	Conditions	Min.	Typ.	Max.	Note
Viewing angle	Deg.	Horizontal (Right)		89		2
		CR=10 (Left)		89		
		Vertical (Up)		89		
		CR=10 (Down)		89		
Contrast Ratio		Normal Direction	3200	4000		3
Response Time	msec	Raising + Falling		8	16	4
Color / Chromaticity Coordinates (CIE)		Red x	-0.05	0.650	+0.05	5
		Red y		0.334		
		Green x		0.305		
		Green y		0.615		
		Blue x		0.150		
		Blue y		0.070		
Color coordinates (CIE) White		White x		0.280		
		White y		0.290		
Center Luminance	Cd/m^2		1040	1300		6
Luminance Uniformity	%		70	75		7
Crosstalk (in 60 Hz)	%				1.5	
Flicker	dB				-20	

Note 1: Measurement method

The LCD module should be stabilized at given temperature for 0.5 hour to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 1 hour in a windless room.



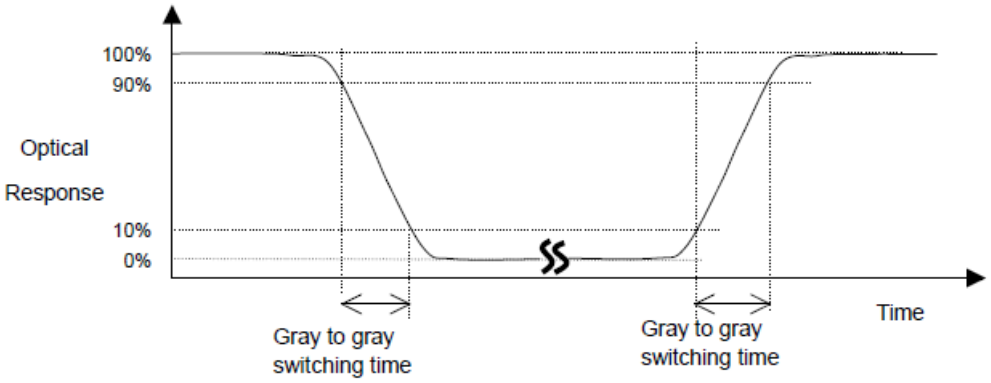
Note 2: Definition of viewing angle



Note 3: Contrast ratio is measured by Minolta CA210

Note 4: Definition of Response time

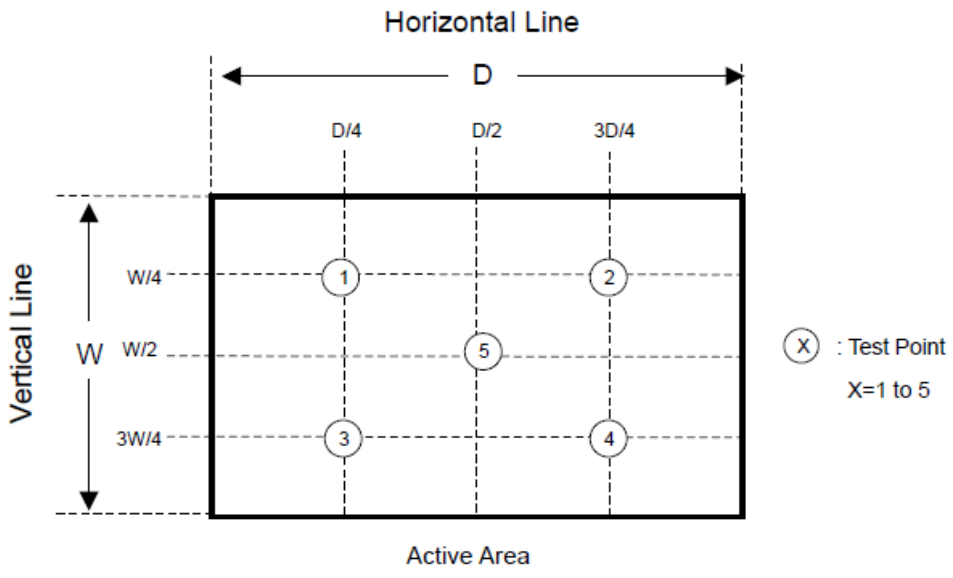
The output signals of photo detector are measured when the input signals are changed from “Full Black” to “Full White” (rising time), and from “Full White” to “Full Black” (falling time), respectively. The response time is interval between the 10% and 90% of amplitudes. Please refer to the figure as below.



Note 5: Color chromaticity and coordinates (CIE) is measured by Minolta CA210

Note 6: Center luminance is measured by Minolta CA210

Note 7: Luminance uniformity of these 5 points is defined as below and measured by Minolta CA210



Uniformity = (Min. Luminance of 5 points) / (Max. Luminance of 5 points)

3. Absolute Maximum Ratings

Absolute maximum ratings of the module are as following:

3.1 TFT LCD module

Items	Symbol	Min	Max	Unit	Conditions
Logic supply voltage	V_{CC}	-0.3	14	Volt	Note 1, 2

3.2 Backlight unit

Items	Symbol	Min	Max	Unit	Conditions
BLU input voltage			26.4	V	

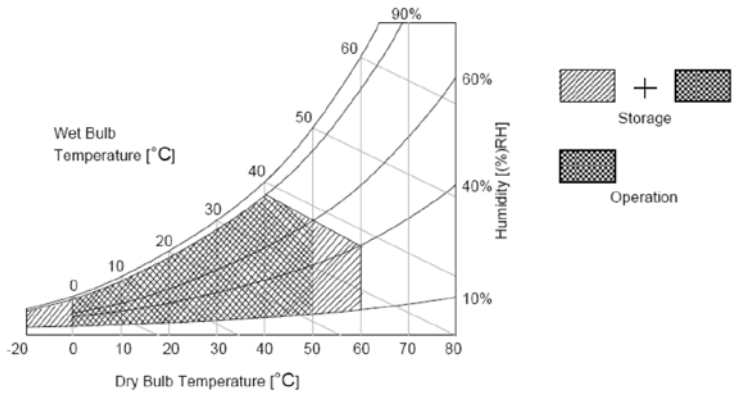
3.3 Environment

Items	Symbol	Values			Unit	Conditions
		Min.	Typ.	Max.		
Operation temperature	T_{OP}	0	-	50	^{0}C	Note 3
Operation Humidity	H_{OP}	10		85	%	
Storage temperature	T_{ST}	-20		60	^{0}C	
Storage Humidity	H_{ST}	5		90	%	

Note 1: With in Ta= 25℃

Note 2: Permanent damage to the device may occur if exceed maximum values

Note 3: For quality performance, please refer to IIS (Incoming Inspection Standard).



4. Electrical Characteristics

4.1 TFT LCD module

4.1.1 Electrical characteristics

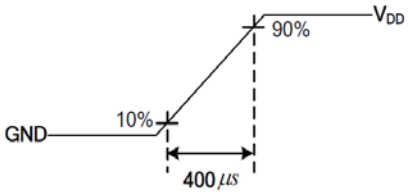
Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max		
LCD							
Power Supply Input Voltage		V_{DD}	10.8	12	13.2	V_{DC}	
Power Supply Input Current		I_{DD}	--	0.48	0.57	A	1
Power Consumption		P_C	--	5.76	6.84	Watt	1
Inrush Current		I_{RUSH}	-	-	3	A	2
Permissible Ripple of Power Supply Input Voltage (for input power=12V)		V_{RP}	--	--	V_{DD} * 5%	mV_{pk-pk}	3
LVDS Interface	Input Differential Voltage	$\lvert V_{ID} \rvert$	200	400	600	mV_{DC}	4
	Differential Input High Threshold Voltage	V_{TH}	+100	--	+300	mV_{DC}	4
	Differential Input Low Threshold Voltage	V_{TL}	-300	--	-100	mV_{DC}	4
	Input Common Mode Voltage	V_{ICM}	1.1	1.25	1.4	V_{DC}	4
CMOS Interface	Input High Threshold Voltage	V_{IH} (High)	2.7	--	3.3	V_{DC}	7
	Input Low Threshold Voltage	V_{IL} (Low)	0	--	0.6	V_{DC}	
Backlight Power Consumption		P_{BL}	--	53.5		W	
Life Time(MTTF)			70000	-	-	--	8

4.1.2 AC characteristics

Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max		
LVDS Interface	Receiver Clock : Spread Spectrum Modulation range	Fclk_ss	Fclk -3%	--	Fclk +3%	MHz	9
	Receiver Clock : Spread Spectrum Modulation frequency	Fss	30	--	200	KHz	9
	Receiver Data Input Margin Fclk = 85 MHz Fclk = 65 MHz	tRMG	 -0.4 -0.5	 -- --	 0.4 0.5	ns	10

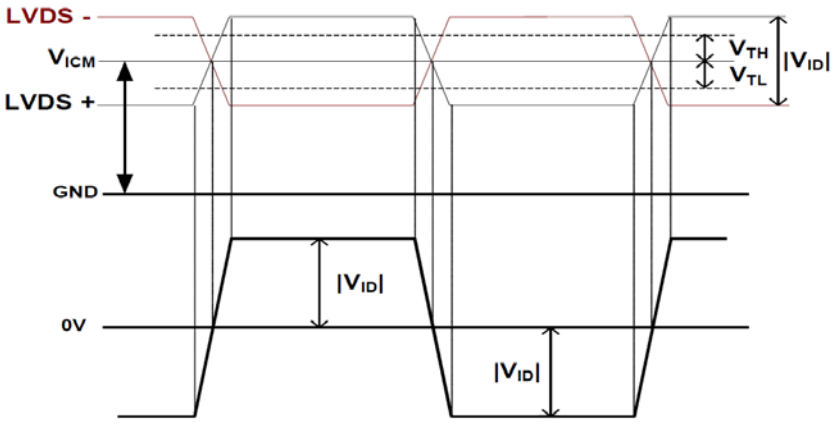
Note :

1. Test Condition:
   (1) V_{DD} = 12.0V
   (2) Fv = Type Timing, 60Hz
   (3) F_{CLK} = Max freq.
   (4) Temperature = 25 ℃
   (5) Test Pattern : White Pattern
2. Measurement condition : Rising time = 400us

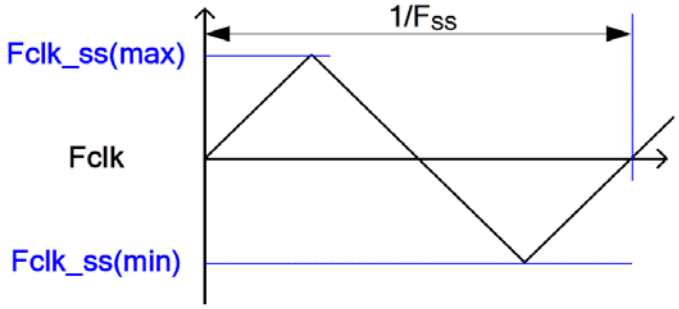


3. Test Condition:
   (1) The measure point of V_{RP} is in LCM side after connecting the System Board and LCM.
   (2) Under Max. Input current spec. condition.

4. V_{ICM} = 1.25V

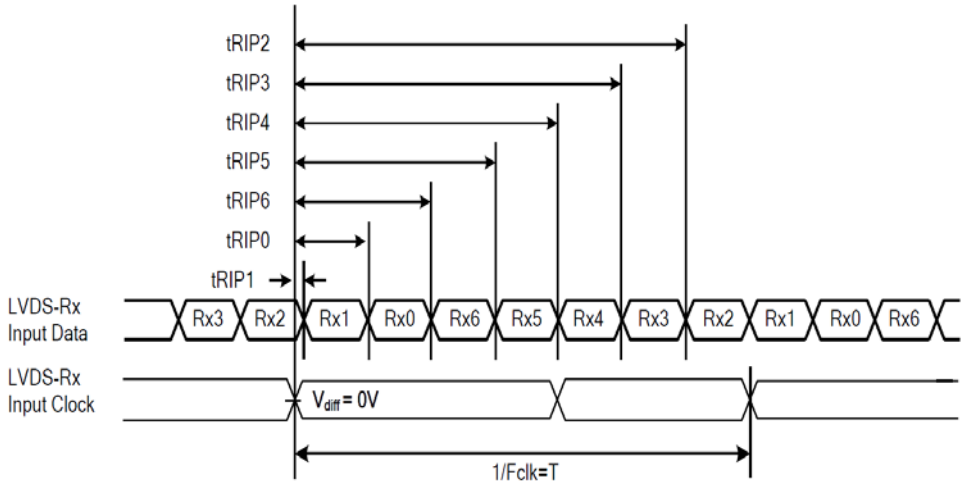


5. Do not attach a conducting tape to lamp connecting wire. If the lamp wire attach to conducting tape, TFT-LCD Module have a low luminance and the inverter has abnormal action because leakage current occurs between lamp wire and conducting tape.
6. The relative humidity must not exceed 80% non-condensing at temperatures of 40℃ or less. At temperatures greater than 40℃, the wet bulb temperature must not exceed 39℃. When operate at high temperatures, the brightness of LED will drop and the life time of LED will be reduced.
7. The measure points of V_{IH} and V_{IL} are in LCM side after connecting the System Board and LCM.
8. The lifetime (MTTF) is defined as the time which luminance of the LED is 50% compared to its original value. [Operating condition: Continuous operating at Ta = 25±2℃]
9. LVDS Receiver Clock SSCG (Spread spectrum clock generator) is defined as below figures



10. Receiver Data Input Margin

Parameter	Symbol	Rating			Unit	Note
		Min	Type	Max		
Input Clock Frequency	Fclk	Fclk (min)	--	Fclk (max)	MHz	**T=1/Fclk**
Input Data Position0	tRIP1	-|tRMG|	0	|tRMG|	ns	
Input Data Position1	tRIP0	T/7-|tRMG|	T/7	T/7+|tRMG|	ns	
Input Data Position2	tRIP6	2T/7-|tRMG|	2T/7	2T/7+|tRMG|	ns	
Input Data Position3	tRIP5	3T/7-|tRMG|	3T/7	3T/7+|tRMG|	ns	
Input Data Position4	tRIP4	4T/7-|tRMG|	4T/7	4T/7+|tRMG|	ns	
Input Data Position5	tRIP3	5T/7-|tRMG|	5T/7	5T/7+|tRMG|	ns	
Input Data Position6	tRIP2	6T/7-|tRMG|	6T/7	6T/7+|tRMG|	ns	



4.2 Backlight unit

	Item	Symbol		Condition	Spec			Unit	Note
					Min	Typ	Max		
1	Input Voltage	VDDB		-	22.8	24	25.2	VDC	-
2	Input Current	I_{DDB}		VDDB=24V	--	2.23	2.48	ADC	1
3	Input Power	P_{DDB}		VDDB=24V	--	53.5	59.5	W	1
4	Inrush Current	I_{RUSH}		VDDB=24V	-	-	7.5	ADC	2
5	On/Off control voltage	V_{BLON}	ON	VDDB=24V	2	-	5.5	VDC	-
			OFF		0	-	0.8		-
6	On/Off control current	I_{BLON}		VDDB=24V	-	-	1.5	mA	-
7	External PWM Control Voltage	V_EPWM	MAX	VDDB=24V	2	-	3.3	VDC	-
			MIN	VDDB=24V	0	-	0.8		-
8	External PWM Control Current	I_EPWM		VDDB=24V	-	-	2	mADC	-
9	External PWM Duty ratio	D_EPWM		VDDB=24V	20	-	100	%	3
10	External PWM Frequency	F_EPWM		VDDB=24V	6000	6500	7000	Hz	-
11	DET status signal	DET	HI	VDDB=24V	Open Collector			VDC	-
			LO		0	-	0.8	VDC	-
12	Input Impedance	Rin		VDDB=24V	300			Kohm	-

Note 1 : Dimming ratio= 100% (MAX) （Ta=25±5℃, Turn on for 45minutes）
Note 2: Measurement condition Rising time = 20ms (VDDB : 10%~90%) and at dimming ration = 100%
Note 3: Less than 20% dimming control is functional well and no backlight shutdown happened

4.3 Interface connector

4.3.1 TFT connector

- LCD connector: FI-RTE51SZ-HF (JAE)
- Matching: FI-RE51HL

PIN	Symbol	Description	PIN	Symbol	Description
1	N.C.	No connection	26	N.C.	No connection
2	N.C.	No connection	27	N.C.	No connection
3	N.C.	No connection	28	CH2_0-	LVDS Channel 2, Signal 0-
4	N.C.	No connection	29	CH2_0+	LVDS Channel 2, Signal 0+
5	BITSEL	LVDS 8/10 bit input selection Open / Low (GND): 8bits High(3.3V): 10bts	30	CH2_1-	LVDS Channel 2, Signal 1-
6	N.C.	N.C.	31	CH2_1+	LVDS Channel 2, Signal 1+
7	LVDS_SEL	Open/High(3.3V) for NS, Low(GND) for JEIDA	32	CH2_2-	LVDS Channel 2, Signal 2-
8	N.C.	No connection	33	CH2_2+	LVDS Channel 2, Signal 2+
9	N.C.	No connection	34	GND	Ground
10	N.C.	No connection	35	CH2_CLK-	LVDS Channel 2, Clock -
11	GND	Ground	36	CH2_CLK+	LVDS Channel 2, Clock +
12	CH1_0-	LVDS Channel 1, Signal 0-	37	GND	Ground
13	CH1_0+	LVDS Channel 1, Signal 0+	38	CH2_3-	LVDS Channel 2, Signal 3-
14	CH1_1-	LVDS Channel 1, Signal 1-	39	CH2_3+	LVDS Channel 2, Signal 3+
15	CH1_1+	LVDS Channel 1, Signal 1+	40	CH2_4-	LVDS Channel 2, Signal 4-
16	CH1_2-	LVDS Channel 1, Signal 2-	41	CH2_4+	LVDS Channel 2, Signal 4+
17	CH1_2+	LVDS Channel 1, Signal 2+	42	N.C.	AUO Internal Use Only
18	GND	Ground	43	N.C.	No connection
19	CH1_CLK-	LVDS Channel 1, Clock -	44	GND	Ground
20	CH1_CLK+	LVDS Channel 1, Clock +	45	GND	Ground
21	GND	Ground	46	GND	Ground
22	CH1_3-	LVDS Channel 1, Signal 3-	47	N.C.	No connection
23	CH1_3+	LVDS Channel 1, Signal 3+	48	V_{DD}	Power Supply, +12V DC Regulated
24	CH1_4-	LVDS Channel 1, Signal 4-	49	V_{DD}	Power Supply, +12V DC Regulated
25	CH1_4+	LVDS Channel 1, Signal 4+	50	V_{DD}	Power Supply, +12V DC Regulated
			51	V_{DD}	Power Supply, +12V DC Regulated

Note: N.C. : please leave this pin unoccupied. It can not be connected by any signal (Low/GND/High).

Note 1: All GND (ground) pins should be connected together and should also be connected to the LCD's metal frame.

Note 2: All V_{DD} (power input) pins should be connected together.

Note 3: All NC (no connection) pins should be open without voltage input.

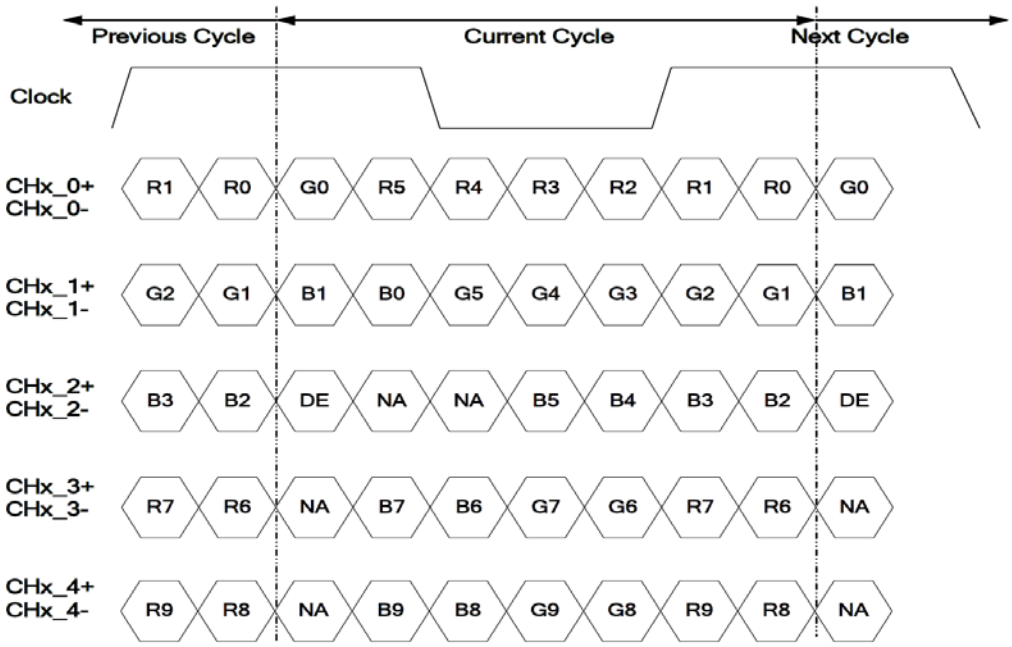
Note4. Aging pattern control

Aging_EN	Mode
H or OPEN	Aging disable
L	Aging enable

Note5. LVDS data format selection

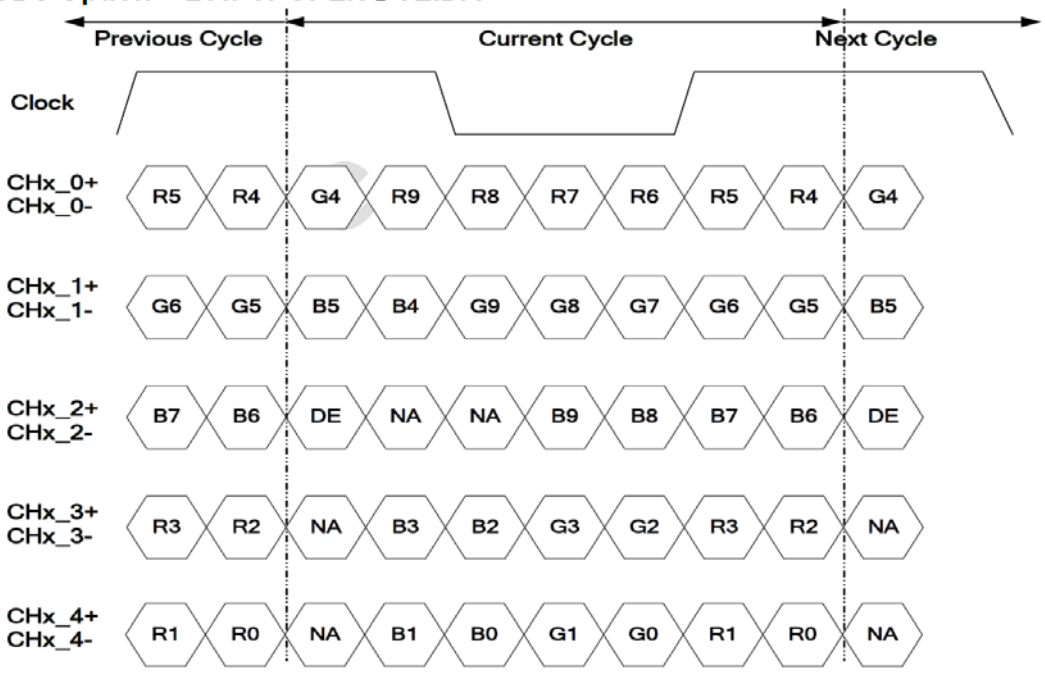
LVDS_SEL	Mode
H	NS
L or OPEN	Jeida

LVDS Option = High➔NS



Note: x = 1, 2, 3, 4…

LVDS Option = Low or OPEN➔JEIDA



Note: x = 1, 2, 3, 4…

4.3.2 Backlight connector

Input Pin Assignment (CN2)

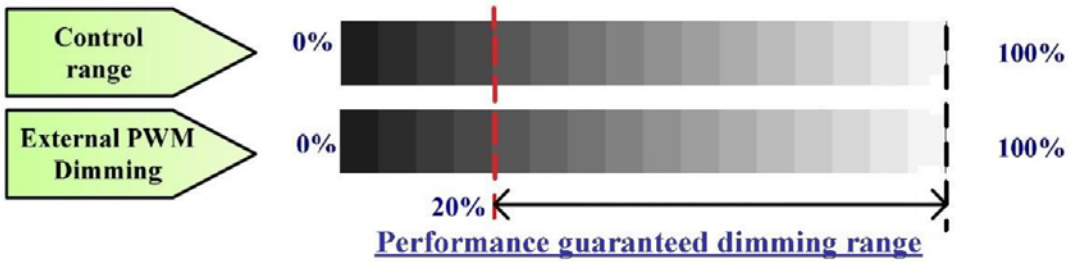
Pin & Connector Assignment:

Connector: JST S14B-PHA-SM3-TB(HF) or equivalent

Matching: PHAR-14

Pin NO	Symbol	Description
1	VIN	DC +24V
2	VIN	DC +24V
3	VIN	DC +24V
4	VIN	DC +24V
5	VIN	DC +24V
6	GND	Ground
7	GND	Ground
8	GND	Ground
9	GND	Ground
10	GND	Ground
11	DET	BLU status detection: Normal: 0~0.8V; Abnormal: open collector (Recommend pull high R>10K, VDD=3.3V)
12	ON / OFF	OFF=0~0.8V/GND; ON=+2.0~5.5V
13	NC	No Connected
14	DIMM	20~100%

PWM Dimming Range:



(Note*) IF External PWM function includes 20% dimming ratio. Judge condition as below:
(1) Backlight module must be lighted ON normally.
(2) All protection function must work normally.
(3) Uniformity and flicker could NOT be guaranteed

4.4 Signal timing specification

This is the signal timing required at the input of the user connector. All of the interface signal timing should be satisfied with the following specifications for its proper operation.

Timing Table (DE only Mode)

Vertical Frequency Range (60Hz)

Signal	Item	Symbol	Min.	Typ.	Max	Unit
Vertical Section	Period	Tv	560	585	940	Th
	Active	Tdisp (v)		540		Th
	Blanking	Tblk (v)	20	45	400	Th
Horizontal Section	Period	Th	1030	1282	1325	Tclk
	Active	Tdisp (h)		960		Tclk
	Blanking	Tblk (h)	70	322	365	Tclk
Clock	Frequency	Fclk=1/Tclk	42	45	48	MHz
Vertical Frequency	Frequency	Fv	47	60	63	Hz
Horizontal Frequency	Frequency	Fh	33.6	35.1	36.6	KHz

Notes:

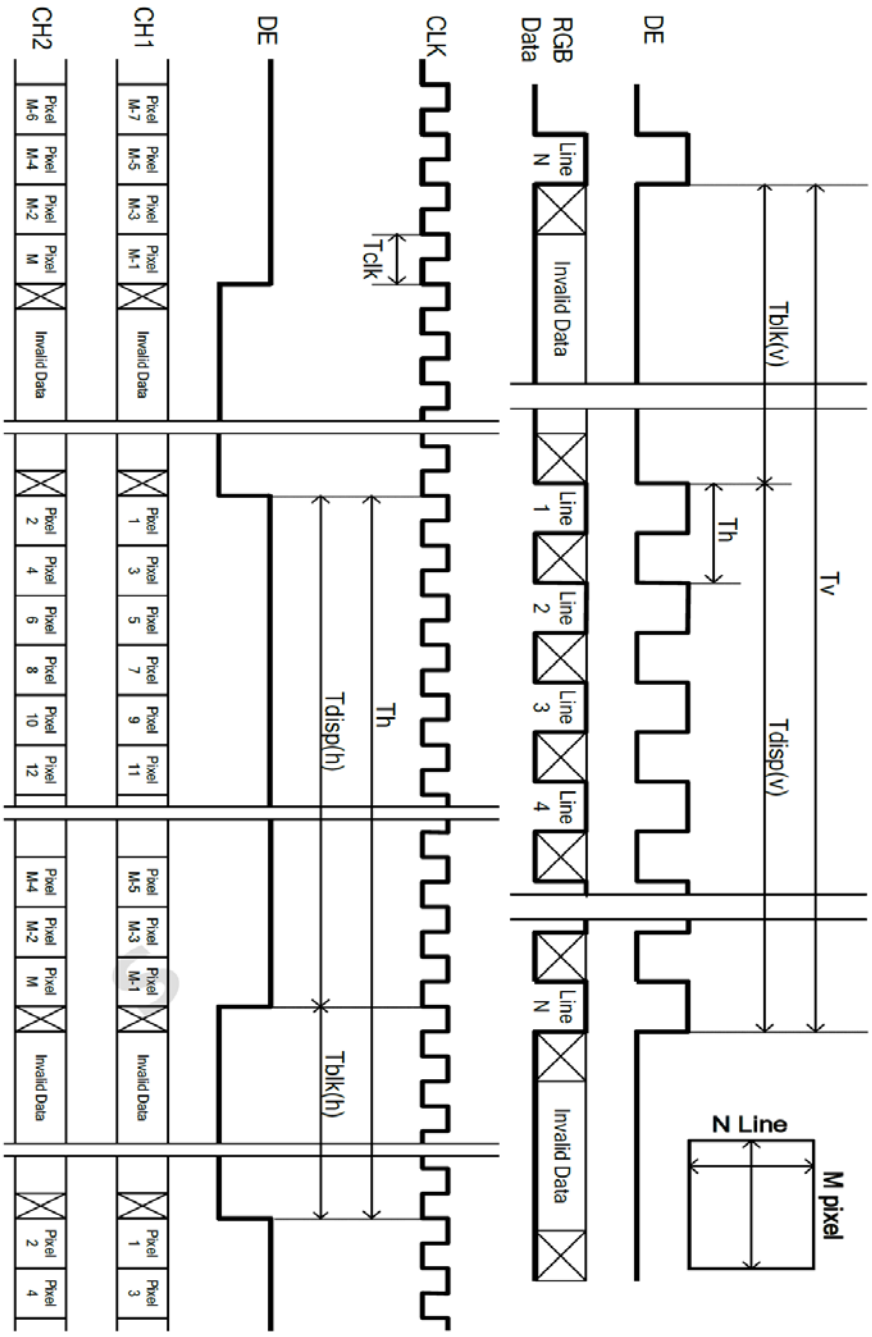
(1) Display position is specific by the rise of DE signal only.
Horizontal display position is specified by the rising edge of 1st DCLK after the rise of 1st DE, is displayed on the left edge of the screen.

(2)Vertical display position is specified by the rise of DE after a "Low" level period equivalent to eight times of horizontal period. The 1st data corresponding to one horizontal line after the rise of 1st DE is displayed at the top line of screen.

(3)If a period of DE "High" is less than 1920 DCLK or less than 540 lines, the rest of the screen displays black.

(4)The display position does not fit to the screen if a period of DE "High" and the effective data period do not synchronize with each other.

4.5 Signal timing waveforms



4.6 Color input data reference

The brightness of each primary color (red, green and blue) is based on the 10 bit gray scale data input for the color; the higher the binary input, the brighter the color. The table below provides a reference for color versus data input.

COLOR DATA REFERENCE

Color		Input Color Data																													
		RED										GREEN										BLUE									
		MSB									LSB	MSB									LSB	MSB									LSB
		R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	G9	G8	G7	G6	G5	G4	G3	G2	G1	G0	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Basic Color	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(1023)	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(1023)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	Blue(1023)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R	RED(000)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED(001)	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

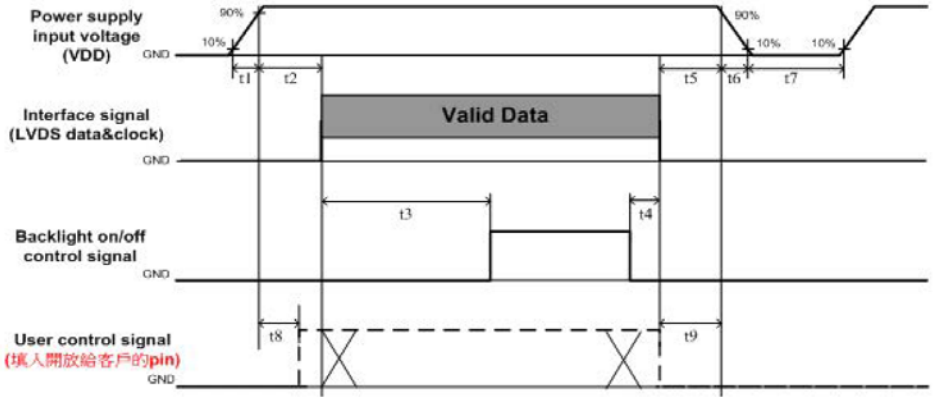
	RED(1022)	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED(1023)	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
G	GREEN(000)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	GREEN(001)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0

	GREEN(1022)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0
	GREEN(1023)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
B	BLUE(000)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	BLUE(001)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

	BLUE(1022)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0
	BLUE(1023)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1

4.7 Power sequence

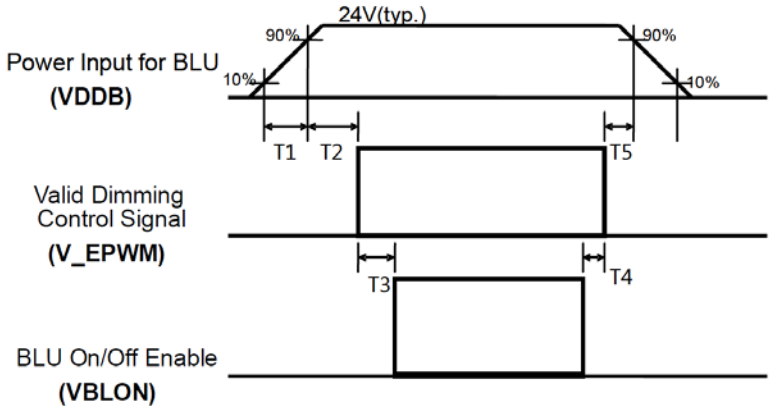
◆ **Power Sequence of LCD**



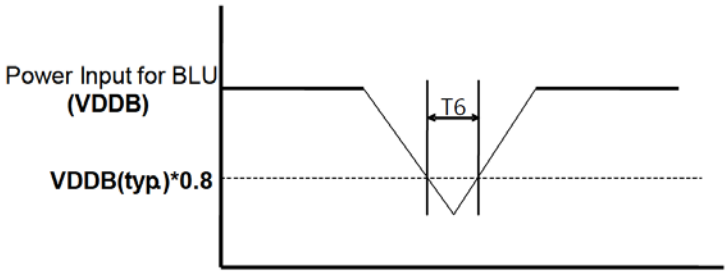
Parameter	Values			Unit
	Min.	Type.	Max.	
t1	0.4	---	30	ms
t2	0.1	---	50	ms
t3	400	---	---	ms
t4	0 *1	---	---	ms
t5	0	---	---	ms
t6	---	---	--- *2	ms
t7	1000 *3	---	---	ms
t8	20 *5	---	50	ms
t9	0	---	---	ms

Note:
(1) t4=0 : concern for residual pattern before BLU turn off.
(2) t6 : voltage of VDD must decay smoothly after power-off. (customer system decide this value)
(3) t7 : When the power supply input voltage(VDD) is off, be sure to pull down the valid and invalid data to 0V.
(4) When user control signal is N.C. (no connection), opened in Transmitted end, t8 timing spec can be negligible.

◆ **Power Sequence of backlight**



Dip Condition



Parameter	Min	Typ	Max	Units
T1	20	-	-	ms
T2	250	-	-	ms
T3	200			ms
T4	0	-	-	ms
T5	0	-	-	ms
T6		-	1000	ms

Note:. T6 describes VDDB dip condition and VDDB couldn't lower than 10% VDDB.

5. Reliability Test

Environment test conditions are listed as following table.

Items	Required Condition	Note
Temperature Humidity Bias (THB)	Ta=40℃, 80%RH, 240hours	
High Temperature Operation (HTO)	Ta= 50℃, 240hours	3
Low Temperature Operation (LTO)	Ta= 0℃, 240hours	
High Temperature Storage (HTS)	Ta= 60℃, 240hours	
Low Temperature Storage (LTS)	Ta= -20℃, 240hours	
Drop Test	Drop Height: 38.1cm, 1corner, 3edge, 6flats, package test	
Thermal Shock Test (TST)	-20℃/30min, 60℃/30min, 100 cycles	
On/Off Test	On/10sec, Off/10sec, 30,000 cycles	
ESD (ElectroStatic Discharge)	Contact Discharge: ± 8KV, 150pF(330Ω) 1sec, 9 points, 25 times/ point.	
	Air Discharge: ± 15KV, 150pF(330Ω) 1sec 9 points, 25 times/ point.	

Note 1: The TFT-LCD module will not sustain damage after being subjected to 100 cycles of rapid temperature change. A cycle of rapid temperature change consists of varying the temperature from 0℃ to 50℃, and back again. Power is not applied during the test. After temperature cycling, the unit is placed in normal room ambient for at least 4 hours before power on.

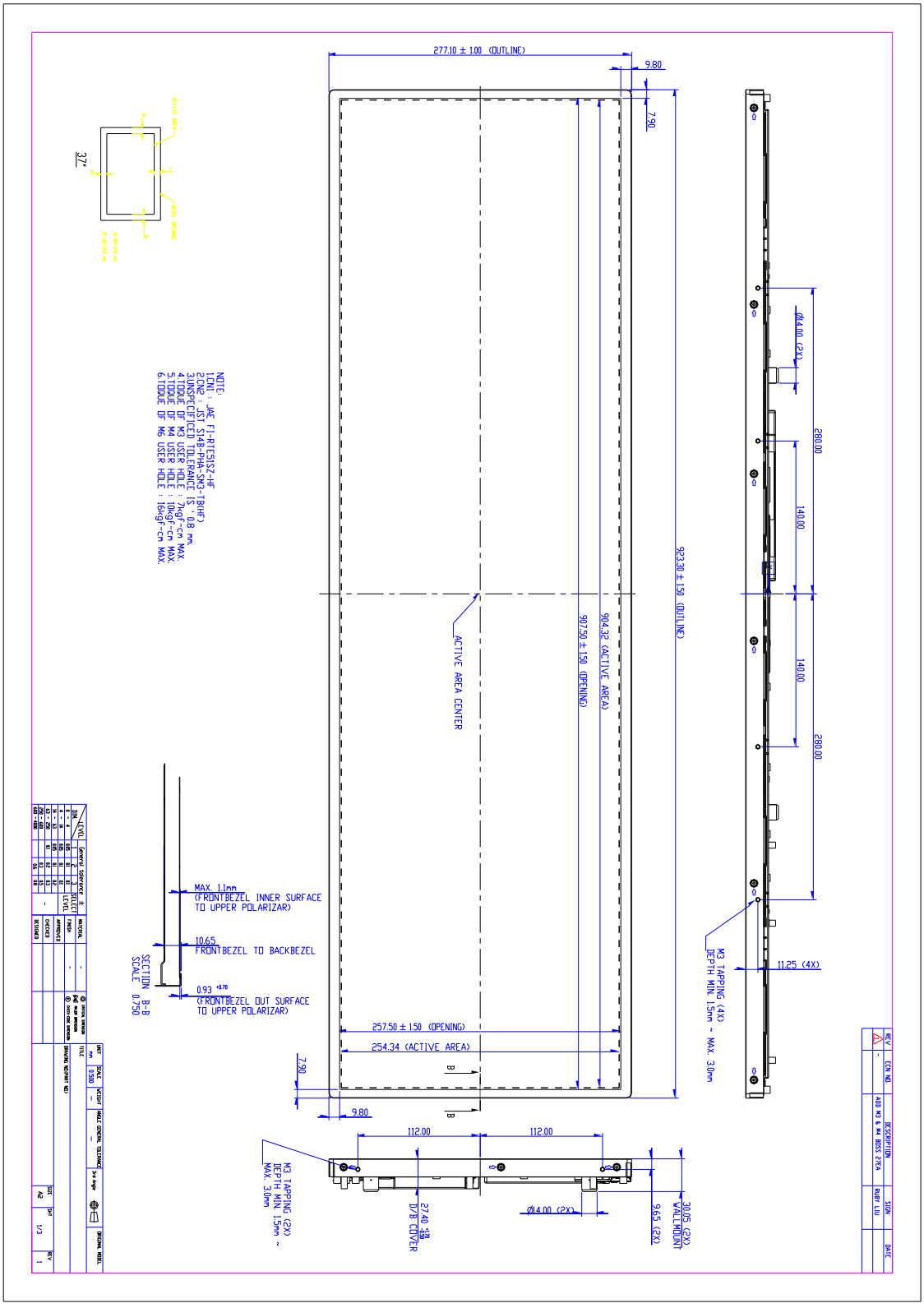
Note 2: According to EN61000-4-2 , ESD class B: Some performance degradation allowed. No data lost. Self-recoverable. No hardware failures.

Note 3: TFT surface.

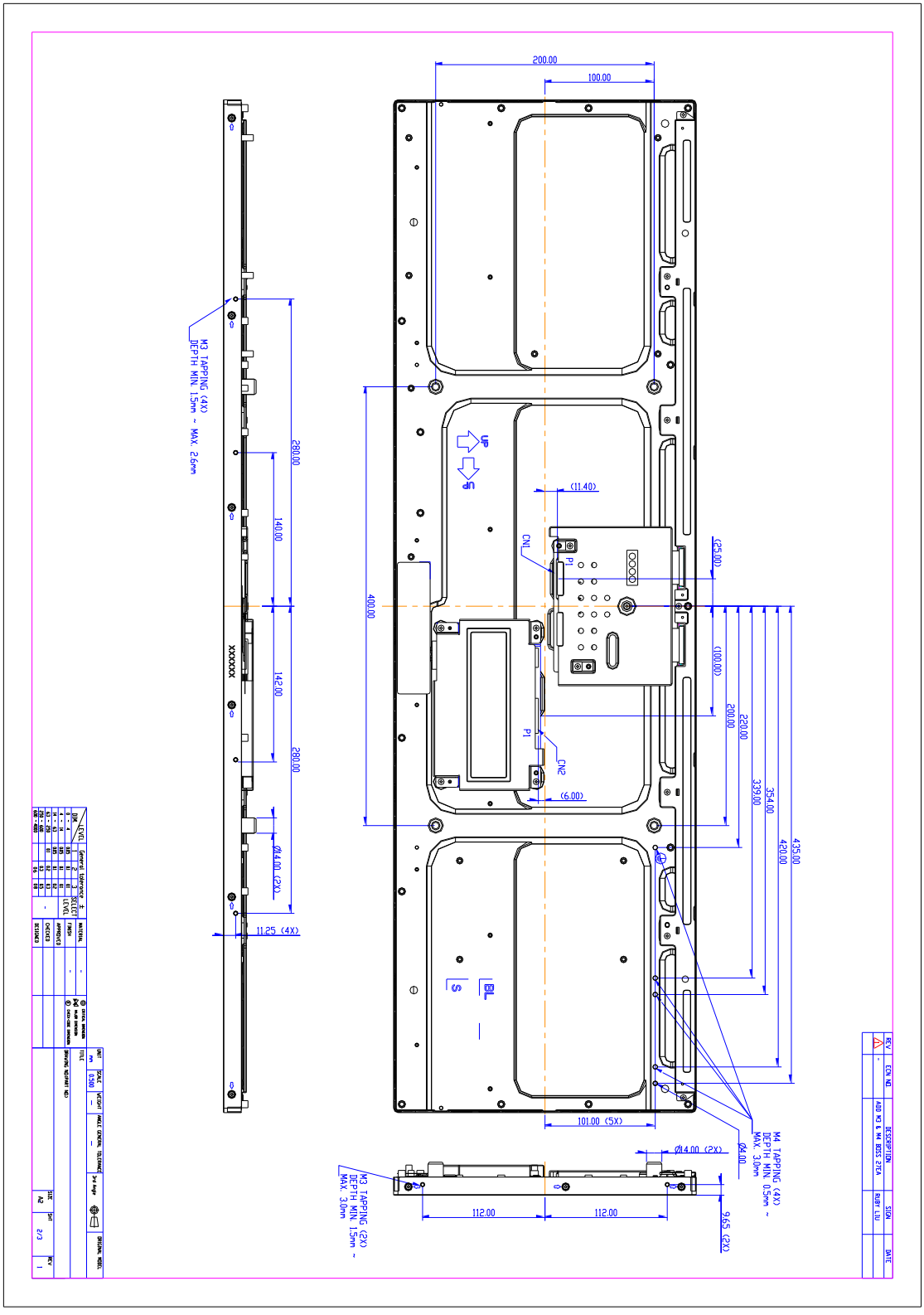
6. Shipping package
(TBD)

7. Mechanical Characteristics

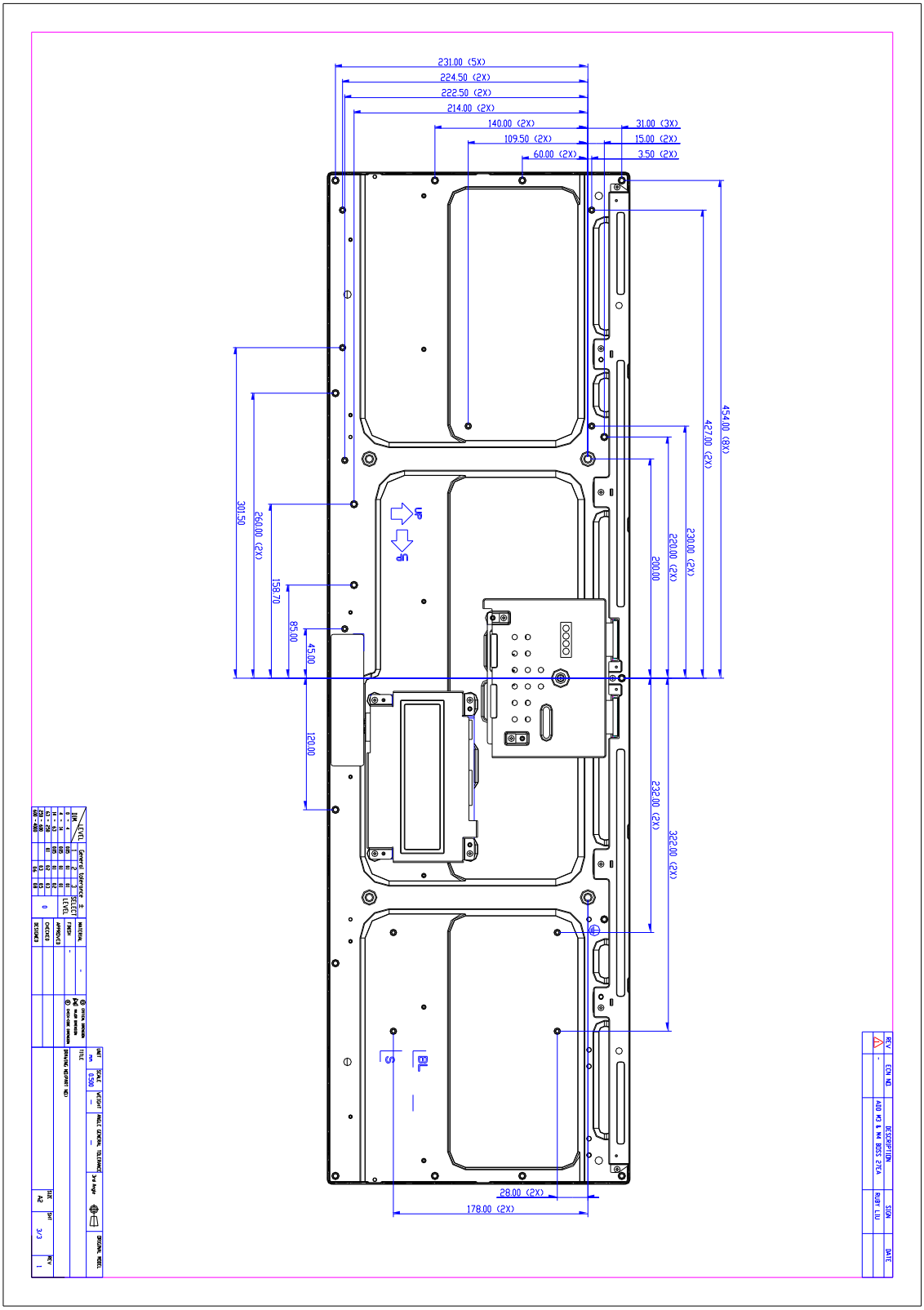
Front View



Back View (I)


200.00
100.00
M3 TAPPING (4X)
DEPTH MIN. 1.5mm ~ MAX. 2.6mm
280.00
140.00
142.00
280.00
Ø4.00 (2X)
11.25 (4X)
XXXXXX
UP
(11.40)
CN1
P1
(25.00)
400.00
(100.00)
200.00
220.00
339.00
354.00
420.00
425.00
P1
CN2
(6.00)
101.00 (5X)
Ø14.00 (2X)
M4 TAPPING (4X)
DEPTH MIN. 0.5mm ~
MAX. 3.0mm
Ø4.00
M3 TAPPING (2X)
DEPTH MIN. 1.5mm ~
MAX. 3.0mm
112.00
112.00
9.65 (2X)

Back View (II)


231.00 (5X)
224.50 (2X)
222.50 (2X)
214.00 (2X)
140.00 (2X)
109.50 (2X)
60.00 (2X)
31.00 (3X)
15.00 (2X)
3.50 (2X)
454.00 (8X)
427.00 (2X)
230.00 (2X)
220.00 (2X)
200.00
301.50
260.00 (2X)
158.70
85.00
45.00
120.00
232.00 (2X)
322.00 (2X)
28.00 (2X)
178.00 (2X)