43” Extreme-wide

High brightness color TFT-LCD module

Customer:

Customer Model name:

Model: VM43

Model control code：VM43BA VB

Date: Oct. 18th, 2019

Version:

Note: This specification is subject to change without notice

Customer： **Approved by ：**   **Date：**

Approved **Date:**	**Prepared** **Date:**

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1. HANDLING PRECAUTIONS

1) Since front polarizer is easily damaged, pay attention not to scratch it.
2) Be sure to turn off power supply when inserting or disconnecting from input connector.
3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
7) Do not open or modify the Module Assembly.
8) Do not press the reflector sheet at the back of the module to any directions.
9) In case if a Module has to be put back into the packing container slot after once it was taken out from the container, do not press the center.
10) After installation of the TFT Module into an enclosure, do not twist nor bend the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.

2. General Description

2.1, Overview

VM43BA VB is a Color Active Matrix Liquid Crystal Display composed of a TFT-LCD panel, a driver circuit, and a backlight system. The screen format is intended to support th 1920(H) x 480 (V) screen and 10-bits/Color. All input signals are 2-channel LVDS interface compatible.

2.2 Features

- High brightness display, 1300nits.
- LED backlight (Edge-type)
- Wide operation temperature (High Tni LC)
- RoHS Compliance

2.3 Application

Industrial Application.

2.4 Display Specifications

Items	Unit	Specification
Screen Diagonal	inch	42.8
Active Area	mm	1039.68 (H) x 259.92 (V)
Pixels H x V	pixels	1920x3(RGB) x 480
Pixels Pitch	mm	0.54(H) x 0.54 (V)
Pixel Arrangement		RGB Vertical stripe
Display mode		Transmissive mode, normally black
White luminance (center)	Cd/m^2	1300 (Typ.)
Contrast ratio		4000 :1(Typ.)
Optical Response Time	msec	8.0 ms (Typ. G to G)
Normal Input Voltage VDD	Volt	12
Power Consumption	Watt	56.792 (typ.) VDD=6.192 W; LED=50.6 W
Weight	Grams	(TBD)
Physical size	mm	1059.48(H) x 283.52(V) x 27.2(D; TBD) (LED driver is NOT included)
Electrical Interface		2 Channel LVDS
Support Colors		RGB 10-bits
Surface Treatment		AG, 3H
Temperature range Operating Storage (Shipping)	 ^0C ^0C	 -10 ~ 50 -20 ~ 60
RoHS Compliance		RoHS Compliance

Note:

(1) D: 56.9 mm (front bezel to Driver Cover)

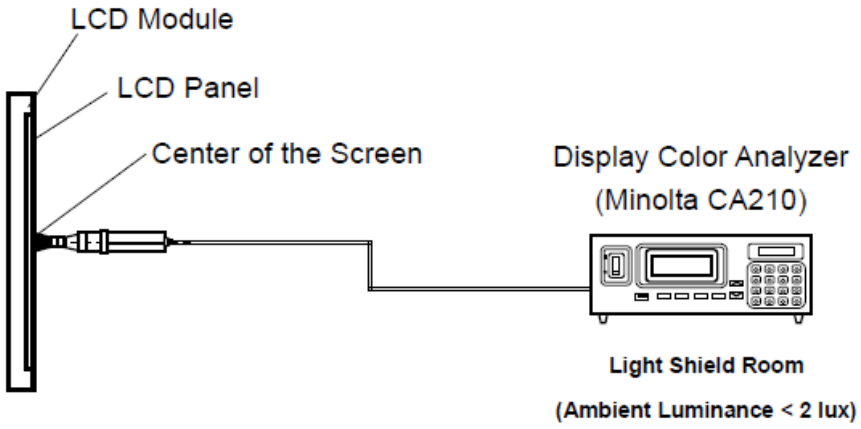
2.5 Optical Characteristics

The following optical characteristics are measured under stable condition at 25 ^{0}C

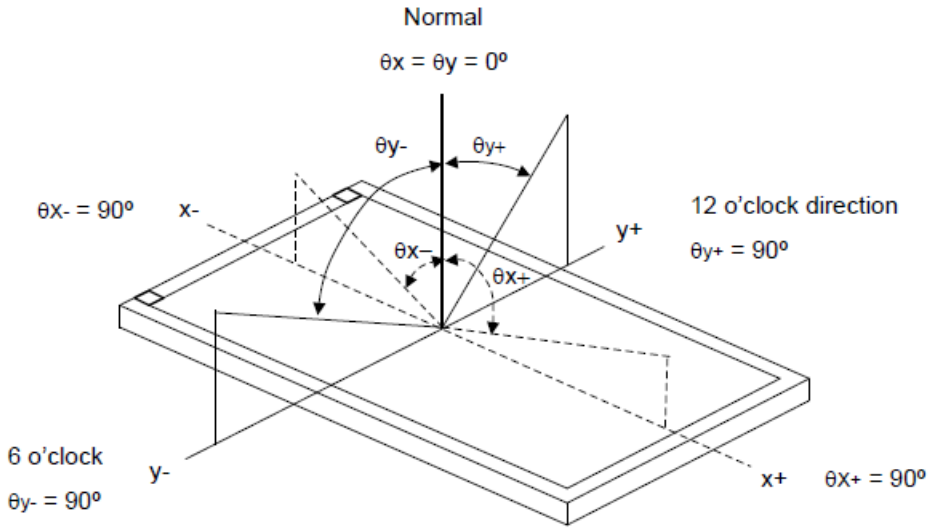
Items	Unit	Conditions	Min.	Typ.	Max.	Note
Viewing angle	Deg.	Horizontal (Right) CR≧20 (Left)	160	178		2
		Vertical (Up) CR≧20 (Down)	160	178		
Contrast Ratio		Normal Direction		4000		3
Response Time	msec	G to G		8		4
Color / Chromaticity Coordinates (CIE)		Red x	-0.05	0.65	+0.05	5
		Red y		0.33		
		Green x		0.31		
		Green y		0.62		
		Blue x		0.15		
		Blue y		0.06		
Color coordinates (CIE) White		White x		0.29		
		White y		0.30		
Center Luminance	Cd/m^2		1000	1300		6
Luminance Uniformity	%			70		7
Crosstalk (in 60 Hz)	%				4.0	

Note 1: Measurement method

The LCD module should be stabilized at given temperature for 0.5 hour to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 1 hour in a windless room.



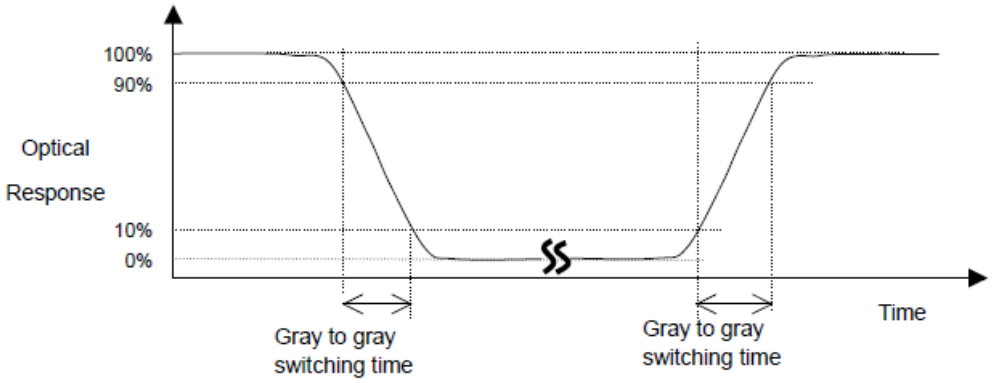
Note 2: Definition of viewing angle



Note 3: Contrast ratio is measured by Minolta CA 210

Note 4: Definition of Response time

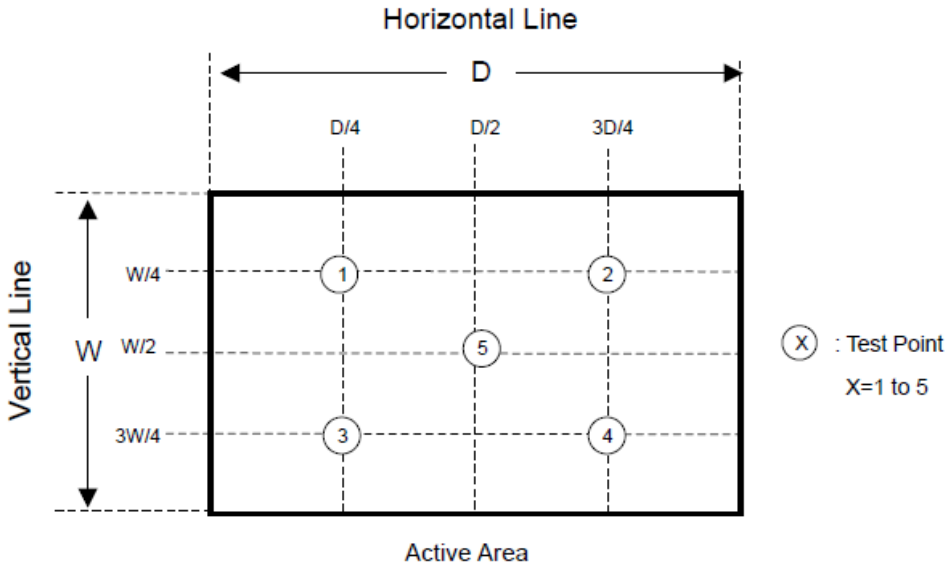
The output signals of photo detector are measured when the input signals are changed from “Full Black” to “Full White” (rising time), and from “Full White” to “Full Black” (falling time), respectively. The response time is interval between the 10% and 90% of amplitudes. Please refer to the figure as below.



Note 5: Color chromaticity and coordinates (CIE) is measured by Minolta CA 210

Note 6: Center luminance is measured by Minolta CA 210

Note 7: Luminance uniformity of these 5 points is defined as below and measured by Minolta CA 210



Uniformity = (Min. Luminance of 5 points) / (Max. Luminance of 5 points)

3. Absolute Maximum Ratings

Absolute maximum ratings of the module are as following:

3.1 TFT LCD Module

Items	Symbol	Min	Max	Unit	Conditions
Power supply voltage	Vcc	-0.3	14		Note 1
Logic/ LCD drive voltage	Vin	-0.3	4.0	Volt	Note 1

3.2 Backlight converter unit

Items	Symbol	Min	Max	Unit	Conditions
Light bar voltage	V_W		(TBD)	V	T=25 ^{0}C
Converter input voltage	V_{BL}	0	28	V	
Control signal level		-0.3	7	V	Note 1, 2

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Function operation should be restricted to the conditions described under Normal Operating Conditions.

3.3 Absolute Ratings of Environment

Items	Symbol	Values			Unit	Conditions
		Min.	Typ.	Max.		
Operation temperature	T_{OP}	-10	-	50	^{0}C	Note 3
Operation Humidity	H_{OP}	5		90	%	
Storage temperature	T_{ST}	-20		60	^{0}C	
Storage Humidity	H_{ST}	5		90	%	

Note 1: With in Ta= 25℃

Note 2: Permanent damage to the device may occur if exceed maximum values

Note 3: For quality performance, please refer to IIS (Incoming Inspection Standard).

4. Electrical characteristics

4.1 Electrical Characteristic

4.1.1: DC Characteristics

Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max		
LCD							
Power Supply Input Voltage		V_{DD}	10.8	12	13.2	V_{DC}	
Power Supply Input Current		I_{DD}	--	0.516	0.619	A	1
Power Consumption		P_C	--	6.192	7.43	Watt	1
Inrush Current		I_{RUSH}	-	-	1.44	A	2
Permissible Ripple of Power Supply Input Voltage (for input power=12V)		V_{RP}	--	--	V_{DD} * 5%	mV_{pk-pk}	3
LVDS Interface	Input Differential Voltage	$\lvert V_{ID} \rvert$	200	400	600	mV_{DC}	4
	Differential Input High Threshold Voltage	V_{TH}	+100	--	+300	mV_{DC}	4
	Differential Input Low Threshold Voltage	V_{TL}	-300	--	-100	mV_{DC}	4
	Input Common Mode Voltage	V_{ICM}	1.1	1.25	1.4	V_{DC}	4
CMOS Interface	Input High Threshold Voltage	V_{IH} (High)	2.7	--	3.3	V_{DC}	7
	Input Low Threshold Voltage	V_{IL} (Low)	0	--	0.6	V_{DC}	

(The backlight power consumption: 56.792W)

4.1.2: AC Characteristics

Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max		
LVDS Interface	Receiver Clock : Spread Spectrum Modulation range	Fclk_ss	Fclk -3%	--	Fclk +3%	MHz	9
	Receiver Clock : Spread Spectrum Modulation frequency	Fss	30	--	200	KHz	9
	Receiver Data Input Margin Fclk = 85 MHz Fclk = 65 MHz	tRMG	 -0.4 -0.5	 -- --	 0.4 0.5	ns	10

Note :

1. Test Condition:

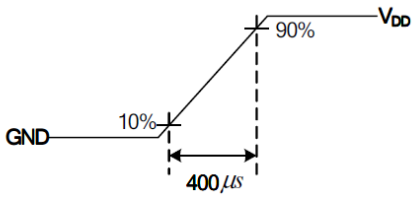
(1) VDD = 12.0V

(2) Fv = 60Hz, 120Hz

(3) Fclk= Max freq.

(4) Temperature = 25 C

2. Measurement condition: Rising time = 400us

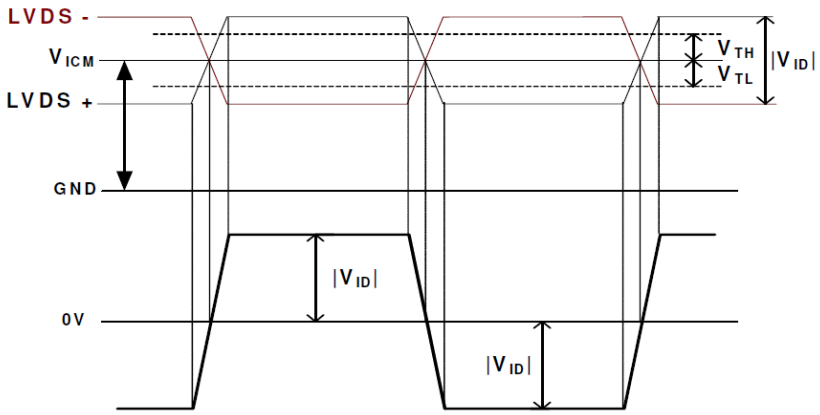


3. Test Condition:

(1) The measure point of VRP is in LCM side after connecting the System Board and LCM.

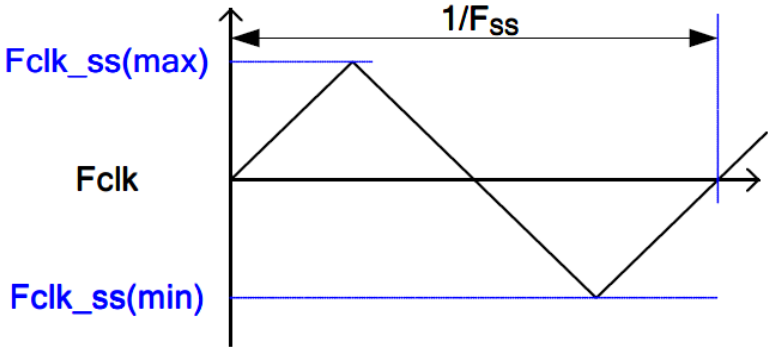
(2) Under Max. Input current spec. condition.

4. V_{ICM} = 1.25V



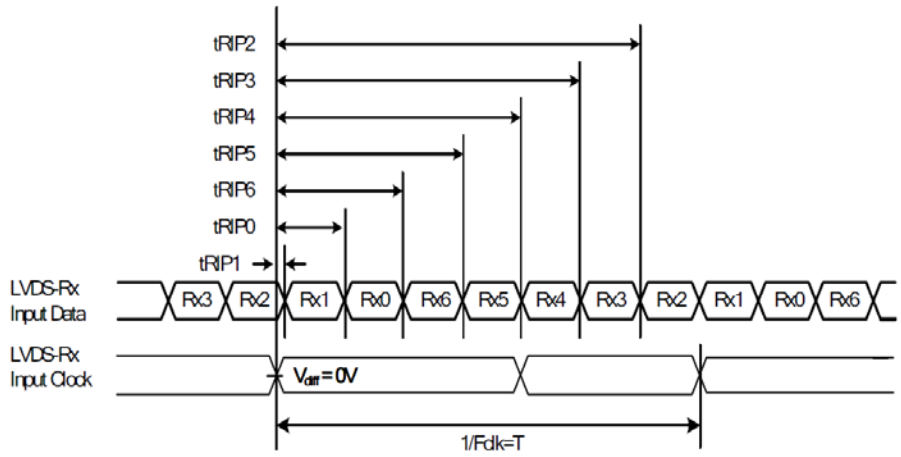
5. The measure points of VIH and VIL are in LCM side after connecting the System Board and LCM.

6. LVDS Receiver Clock SSCG (Spread spectrum clock generator) is defined as below figures.



7. Receiver Data Input Margin

Parameter	Symbol	Rating			Unit	Note
		Min	Type	Max		
Input Clock Frequency	Fclk	Fclk (min)	--	Fclk (max)	MHz	**T=1/Fclk**
Input Data Position0	tRIP1	-|tRMG|	0	|tRMG|	ns	
Input Data Position1	tRIP0	T/7-|tRMG|	T/7	T/7+|tRMG|	ns	
Input Data Position2	tRIP6	2T/7-|tRMG|	2T/7	2T/7+|tRMG|	ns	
Input Data Position3	tRIP5	3T/7-|tRMG|	3T/7	3T/7+|tRMG|	ns	
Input Data Position4	tRIP4	4T/7-|tRMG|	4T/7	4T/7+|tRMG|	ns	
Input Data Position5	tRIP3	5T/7-|tRMG|	5T/7	5T/7+|tRMG|	ns	
Input Data Position6	tRIP2	6T/7-|tRMG|	6T/7	6T/7+|tRMG|	ns	

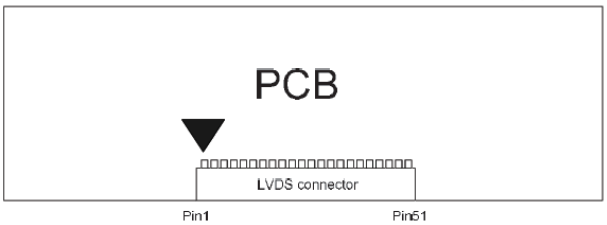


4.2 Interface Connections

LCD connector: FI-RTE51SZ-HF (JAE, LVDS connector)

PIN	Symbol	Description	Note	PIN	Symbol	Description	Note
1	N.C.	No connection	2	26	N.C.	No connection	2
2	SCL	I2C Serial Clock	3&5	27	N.C.	No connection	2
3	WP	EEPROM Write Protection High(3.3V) for Writable, Open/Low(GND) for Protection	3&7	28	CH2_0-	LVDS Channel 2, Signal 0-	
4	SDA.	I2C Serial Data	3&5	29	CH2_0+	LVDS Channel 2, Signal 0+	
5	BITSEL	LVDS 8/10bit input selection Open/ Low (GND): 8bits High (3.3V): 10bit	3&6	30	CH2_1-	LVDS Channel 2, Signal 1-	
6	N.C.	No connection	2	31	CH2_1+	LVDS Channel 2, Signal 1+	
7	LVDS_SEL	Open/ High (3.3V) for NS Low (GND) for JEIDA	3&4	32	CH2_2-	LVDS Channel 2, Signal 2-	
8	N.C.	No connection	2	33	CH2_2+	LVDS Channel 2, Signal 2+	
9	N.C.	No connection	2	34	GND	Ground	
10	N.C.	No connection	2	35	CH2_CLK-	LVDS Channel 2, Clock -	
11	GND	Ground		36	CH2_CLK+	LVDS Channel 2, Clock +	
12	CH1_0-	LVDS Channel 1, Signal 0-		37	GND	Ground	
13	CH1_0+	LVDS Channel 1, Signal 0+		38	CH2_3-	LVDS Channel 2, Signal 3-	
14	CH1_1-	LVDS Channel 1, Signal 1-		39	CH2_3+	LVDS Channel 2, Signal 3+	
15	CH1_1+	LVDS Channel 1, Signal 1+		40	CH2_4-	LVDS Channel 2, Signal 4-	
16	CH1_2-	LVDS Channel 1, Signal 2-		41	CH2_4+	LVDS Channel 2, Signal 4+	
17	CH1_2+	LVDS Channel 1, Signal 2+		42	N.C.	No connection	2
18	GND	Ground		43	N.C.	No connection	2
19	CH1_CLK-	LVDS Channel 1, Clock -		44	GND	Ground	
20	CH1_CLK+	LVDS Channel 1, Clock +		45	GND	Ground	
21	GND	Ground		46	GND	Ground	
22	CH1_3-	LVDS Channel 1, Signal 3-		47	N.C.	No connection	2
23	CH1_3+	LVDS Channel 1, Signal 3+		48	V_{DD}	Power Supply Input Voltage	
24	CH1_4-	LVDS Channel 1, Signal 4-		49	V_{DD}	Power Supply Input Voltage	
25	CH1_4+	LVDS Channel 1, Signal 4+		50	V_{DD}	Power Supply Input Voltage	
				51	V_{DD}	Power Supply Input Voltage	

Note1. Pin number start from the left side as the following figure.



Note2. Please leave this pin unoccupied. It can not be connected by any signal (Low/GND/High).

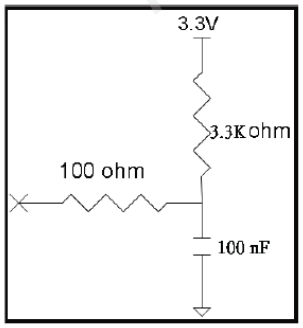
Note3. Input control signal threshold voltage definition

Item	Symbol	Min.	Typ.	Max.	Unit
Input High Threshold Voltage	VIH	2.7	-	3.6	V
Input Low Threshold Voltage	VIL	0	-	0.6	V

Note4. LVDS data format selection

LVDS_SEL	Mode
H or OPEN	NS
L	Jeida

Input equivalent impedance of LVDE_SEL pin

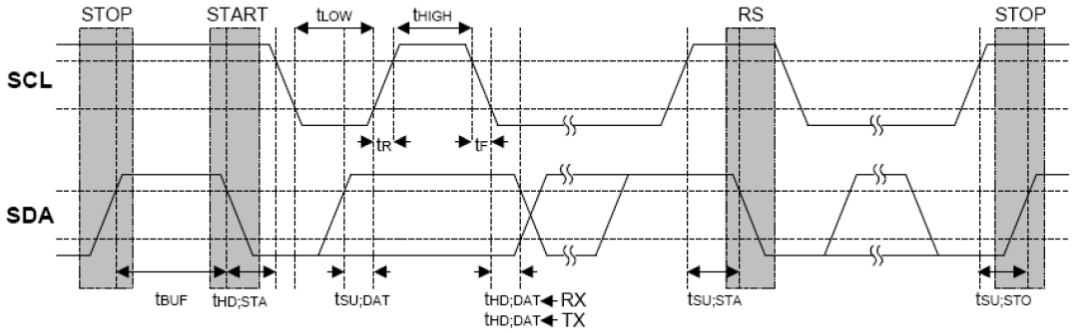


Note5. I2C Data and Clock

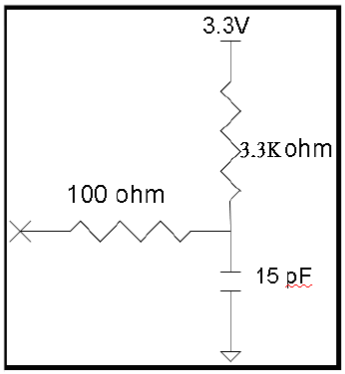
I2C Data and Clock timing

Symbol	Parameter	Standard Mode		Fast Mode		Unit
		Min.	Max	Min	Max	
fSCL	SCL Clock Frequency		100		400	KHz
tBUF	Bus Free Between a STOP and START Condition	4.7		1.3		us

tHD;STA	Hold Time for START Condition		4.0		0.6		us
tLOW	LOW Period of The SCL Clock		4.7		1.3		us
tHIGH	HIGH Period of The SCL Clock		4.0		0.6		us
tSU;STA	Set-up Time for a Repeated START Condition		4.7		0.6		us
tHD;DAT	Data Hold Time	Transmitter	0.1		0.1	0.9	us
		Receiver	0		0		
tSU;DAT	Data Set-up Time		250		100		ns
Tr	Rise Time of Both SDA and SCL Signals			1000		300	ns
tf	Fall Time of Both SDA and SCL Signals			300		300	ns
tSU;STO	Set-up Time for STOP Condition		4.0		0.6		us
tSP	Pulse Width of spikes which must be suppressed by the input filter		0	50	0	50	ns
CI	Capacitance for each Bus Pin		-	10		10	pF
Cb	Capacitive load for each Bus Line		-	400		400	pF



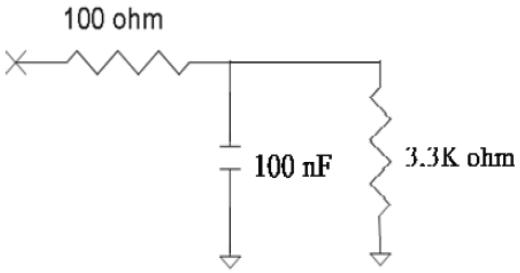
Input equivalent impedance of SDA/SCL pin



Note6. Data Bit mode format selection

BIT_SEL	Mode
H	10Bit
L or OPEN	8Bit

Input equivalent impedance of BIT_SEL pin

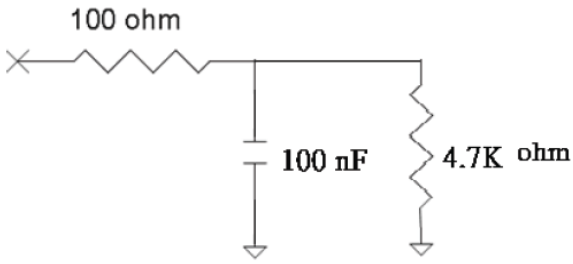


Note7. Write Protection

Mode selection

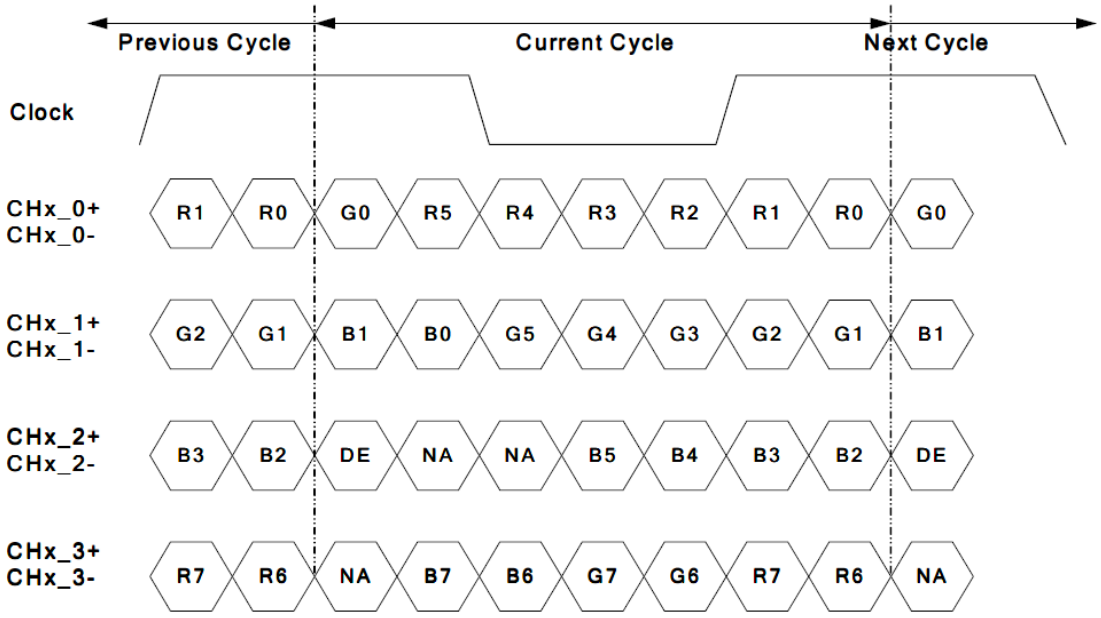
WP	Note
L or OPEN	Protection
H	Writable

Input equivalent impedance of WP pin



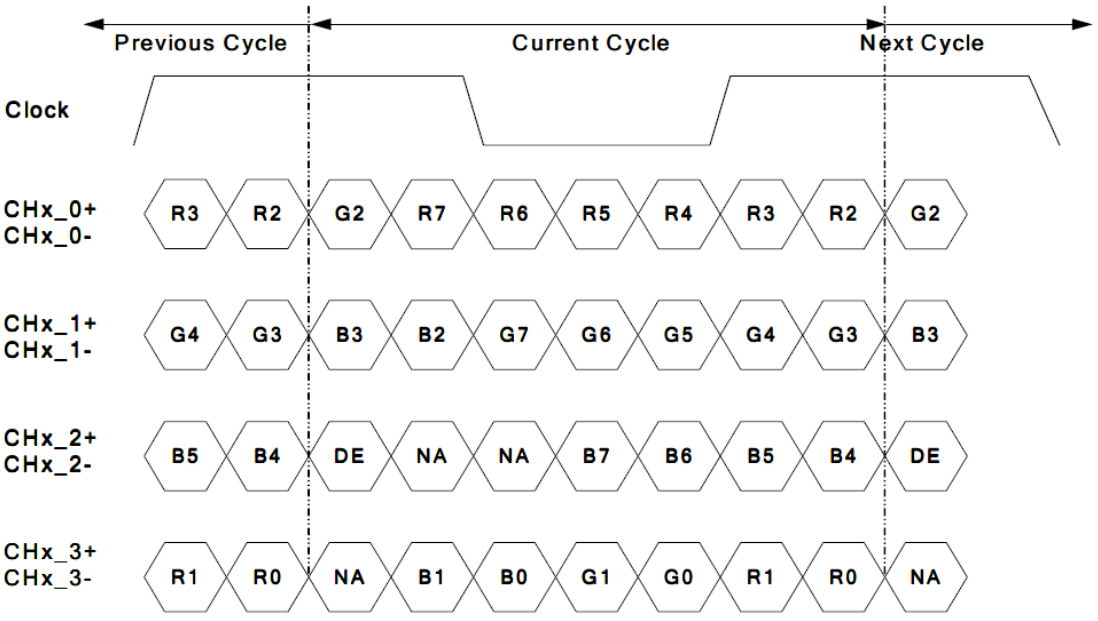
LVDS Option for 8bit

LVDS Option = High/Open_NS



Note: x = 1, 2, 3, 4…

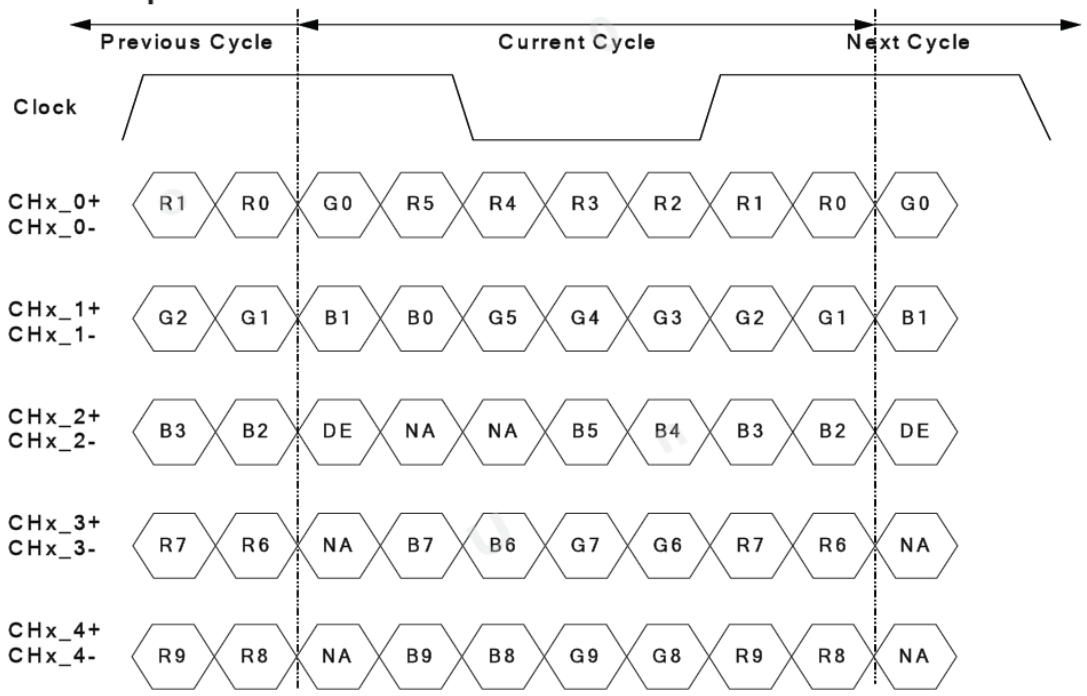
LVDS Option = Low_JEIDA



Note: x = 1, 2, 3, 4…

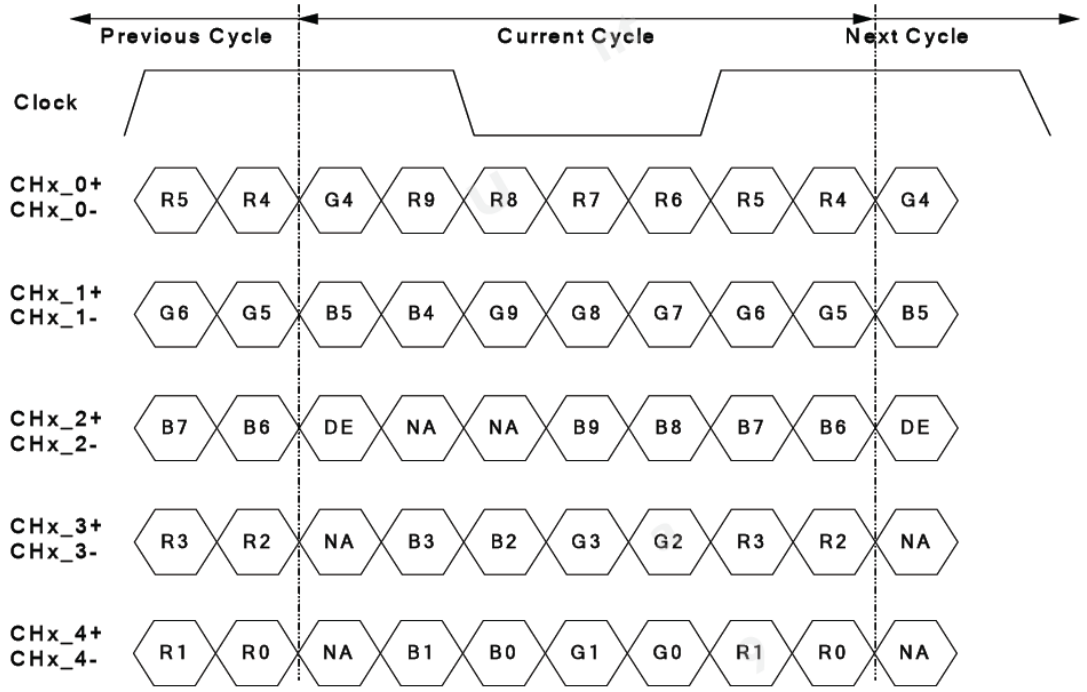
LVDS Option for 10bit

■ LVDS Option NS



Note: x = 1, 2, 3, 4...

■ LVDS Option JEIDA



Note: x = 1, 2, 3, 4...

4.3 Signal Timing Specification

This is the signal timing required at the input of the user connector. All of the interface signal timing should be satisfied with the following specifications for its proper operation.

Timing Table (DE only Mode)

Vertical Frequency Range (60Hz)

Signal	Item	Symbol	Min.	Typ.	Max	Unit
Vertical Section	Period	Tv	500	585	860	Th
	Active	Tdisp (v)	480			
	Blanking	Tblk (v)	20	105	380	Th
Horizontal Section	Period	Th	1200	1282	1325	Tclk
	Active	Tdisp (h)	960			
	Blanking	Tblk (h)	240	322	365	Tclk
Clock	Frequency	Fclk=1/Tclk	42	45	48	MHz
Vertical Frequency	Frequency	Fv	47	60	63	Hz
Horizontal Frequency	Frequency	Fh	33.6	35.1	36.6	KHz

Notes:

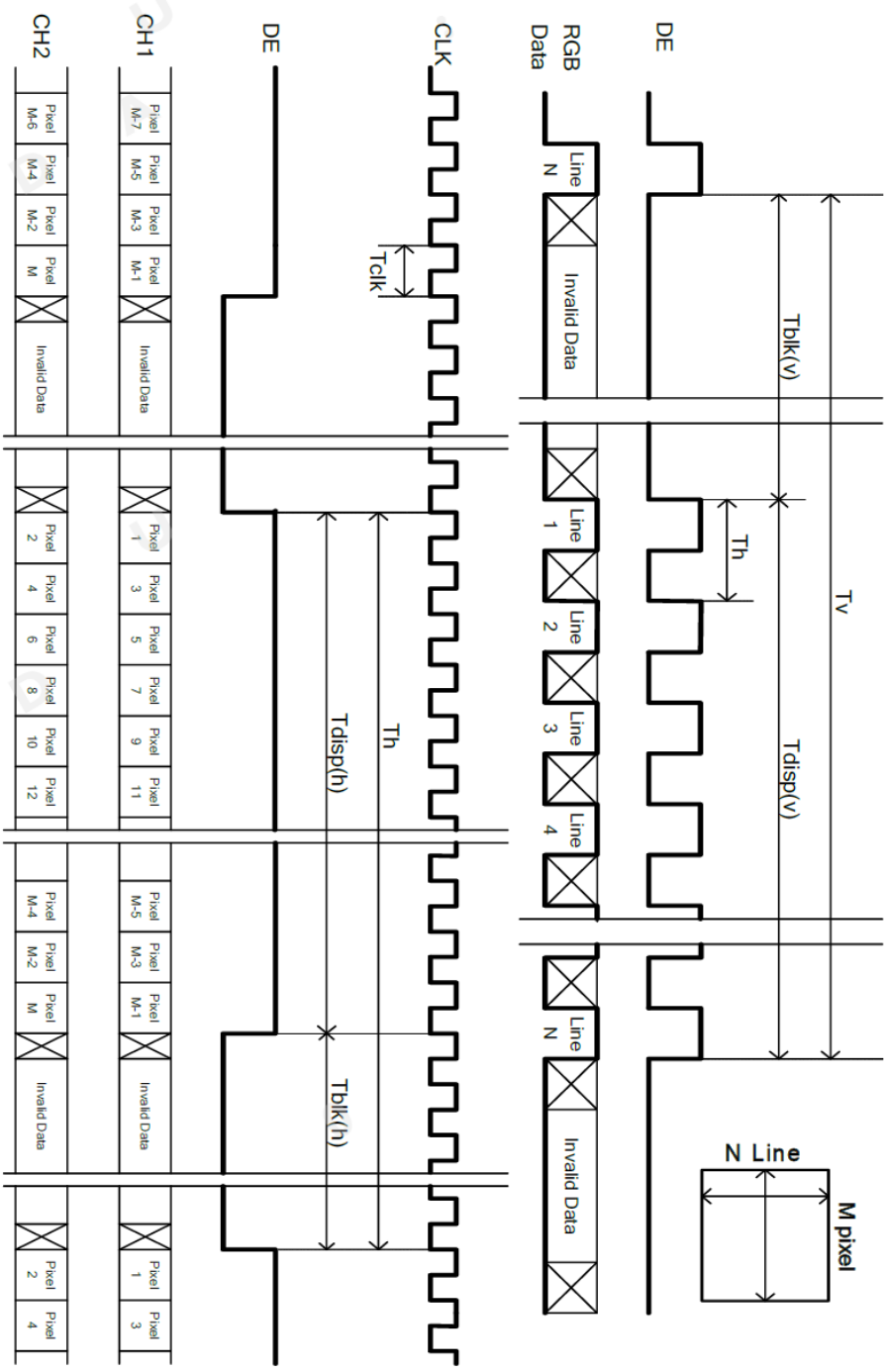
(1) Display position is specific by the rise of DE signal only. Horizontal display position is specified by the rising edge of 1st DCLK after the rise of 1st DE, is displayed on the left edge of the screen.

(2)Vertical display position is specified by the rise of DE after a “Low” level period equivalent to eight times of horizontal period. The 1st data corresponding to one horizontal line after the rise of 1st DE is displayed at the top line of screen.

(3)If a period of DE “High” is less than 1920 DCLK or less than 480 lines, the rest of the screen displays black.

(4)The display position does not fit to the screen if a period of DE “High” and the effective data period do not synchronize with each other.

4.4 Signal Timing Waveforms



4.5 Color Input Data Reference

The brightness of each primary color (red, green and blue) is based on the 10 bit gray scale data input for the color; the higher the binary input, the brighter the color. The table below provides a reference for color versus data input.

COLOR DATA REFERENCE

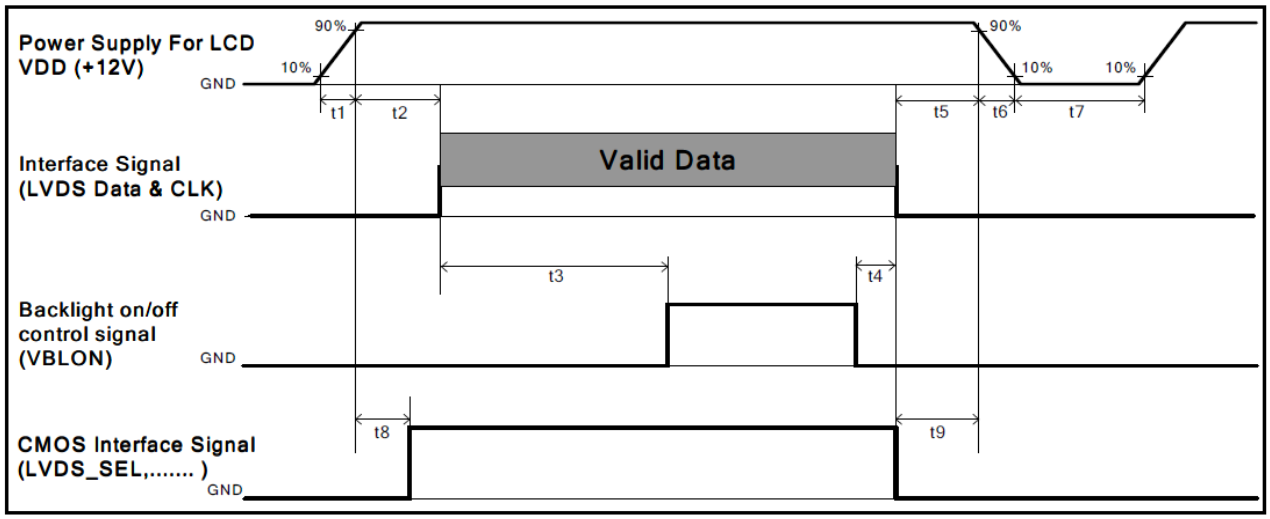
Color		Input Color Data																													
		RED										GREEN										BLUE									
		MSB									LSB	MSB									LSB	MSB									LSB
		R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	G9	G8	G7	G6	G5	G4	G3	G2	G1	G0	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Basic Color	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(1023)	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(1023)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	Blue(1023)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R	RED(000)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED(001)	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	RED(1022)	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED(1023)	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
G	GREEN(000)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	GREEN(001)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0

	GREEN(1022)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0
	GREEN(1023)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
B	BLUE(000)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	BLUE(001)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

	BLUE(1022)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0
	BLUE(1023)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1

4.6 Power Sequence for LCD



Parameter	Values			Unit
	Min.	Type.	Max.	
t1	0.4	---	30	ms
t2	0.1	---	**50**	ms
t3	**450**	---	---	ms
t4	0 *1	---	---	ms
t5	0	---	---	ms
t6	---	---	--- *2	ms
t7	500	---	---	ms
t8	10 *3	---	50	ms
t9	0	---	---	ms

Note:

(1) t4=0 : concern for residual pattern before BLU turn off.

(2) t6 : voltage of VDD must decay smoothly after power-off. (customer system decide this value)

(3) When CMOS Interface signal is N.C. (no connection), opened in Transmitted end, t8 timing spec can be negligible.

4.7 Backlight Specification (independent driver board)

The backlight unit contains edge type light bar.

（Ta=25±5℃, Turn on for 15minutes）

Parameter	Symbol	Min	Typ.	Max	Unit	Remarks (Test condition)
Input Voltage & Current	Vin		24.0		VDC	Vin=24V, Dim=max
	Iin		2.11		A	
Input power	Pin		50.6		W	
On/Off control	ON/OFF		3	5	VDC	ON state
		-0.3		0.7		OFF state
Dimming control	DIMM	180	200	220	Hz	PWM
Backlight lifetime	hrs		50,000			

Note 1 : Dimming ratio= 100% (MAX)（Ta=25±5℃, Turn on for 15minutes）

Note 2: Measurement condition Rising time = 20ms (VDDB: 10%~90%);

Note 3: When BLU off (VDDB = 24V, VBLON = 0V), IDDB (max) = 0.02A

Note 5: Less than 5% dimming control is functional well and no backlight shutdown happened

4.7.2: Input Pin Assignment

Pin & Connector Assignment: Connector: CviLux CI0114M1HRL-NH or equivalent

Pin NO	Symbol	Description
1	VIN	DC +24V
2	VIN	DC +24V
3	VIN	DC +24V
4	VIN	DC +24V
5	VIN	DC +24V
6	GND	Ground
7	GND	Ground
8	GND	Ground
9	GND	Ground
10	GND	Ground
11	DET	BLU status detection: Normal: GND; Abnormal: Open collector
12	ON / OFF	OFF=0V; ON=+5V
13	NC	No connection
14	DIMM	External PWM (20%~100% Duty, open for 100%)

Pin & Connector Assignment: Connector: CviLux CI0112M1HRL-NH or equivalent

Pin NO	Symbol	Description
1	VIN	DC +24V
2	VIN	DC +24V
3	VIN	DC +24V
4	VIN	DC +24V
5	VIN	DC +24V
6	GND	Ground
7	GND	Ground
8	GND	Ground
9	GND	Ground
10	GND	Ground
11	NC	No connection
12	NC	No connection

5.0 Reliability Test

Environment test conditions are listed as following table.

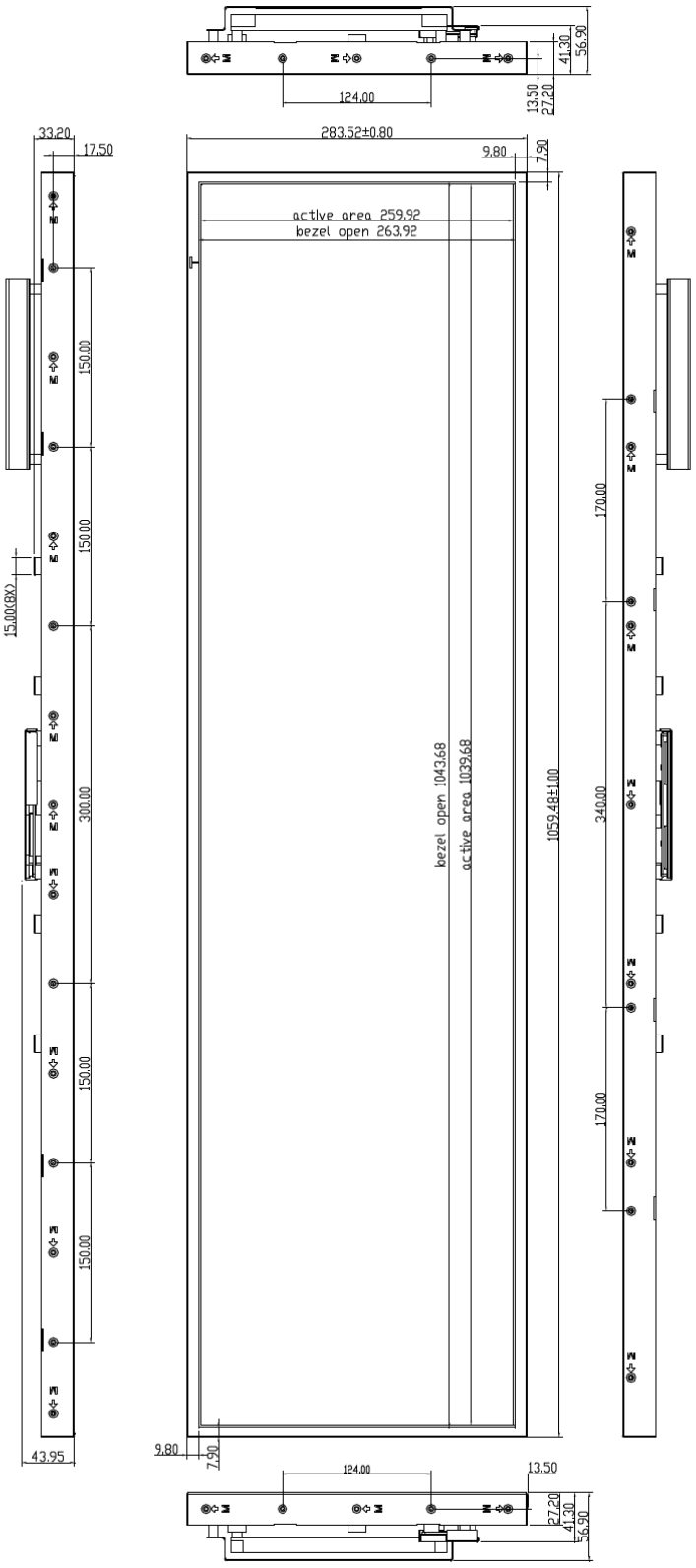
Items	Required Condition	Note
Temperature Humidity Bias (THB)	Ta= 50℃, 80%RH, 300hours	
High Temperature Operation (HTO)	Ta= 50℃, 50%RH, 300hours	3
Low Temperature Operation (LTO)	Ta= -10℃, 300hours	
High Temperature Storage (HTS)	Ta= 60℃, 300hours	
Low Temperature Storage (LTS)	Ta= -20℃, 300hours	
Vibration test (non-operation)	Wave form: random Vibration level: 1.0G RMS Bandwidth: 10-300Hz, Duration: X, Y, Z 10min per axes X,Y,Z : Vertical	
Drop Test	Height: 25.4 cm, package test	
Thermal Shock Test (TST)	-20℃/30min, 60℃/30min, 100 cycles	1
On/Off Test	On/10sec, Off/10sec, 30,000 cycles	
ESD (Electrostatic Discharge)	Contact Discharge: ± 8KV, 150pF(330Ω) 1sec, 9 points, 25 times/ point.	2
	Air Discharge: ± 15KV, 150pF(330Ω) 1sec 9 points, 25 times/ point.	2

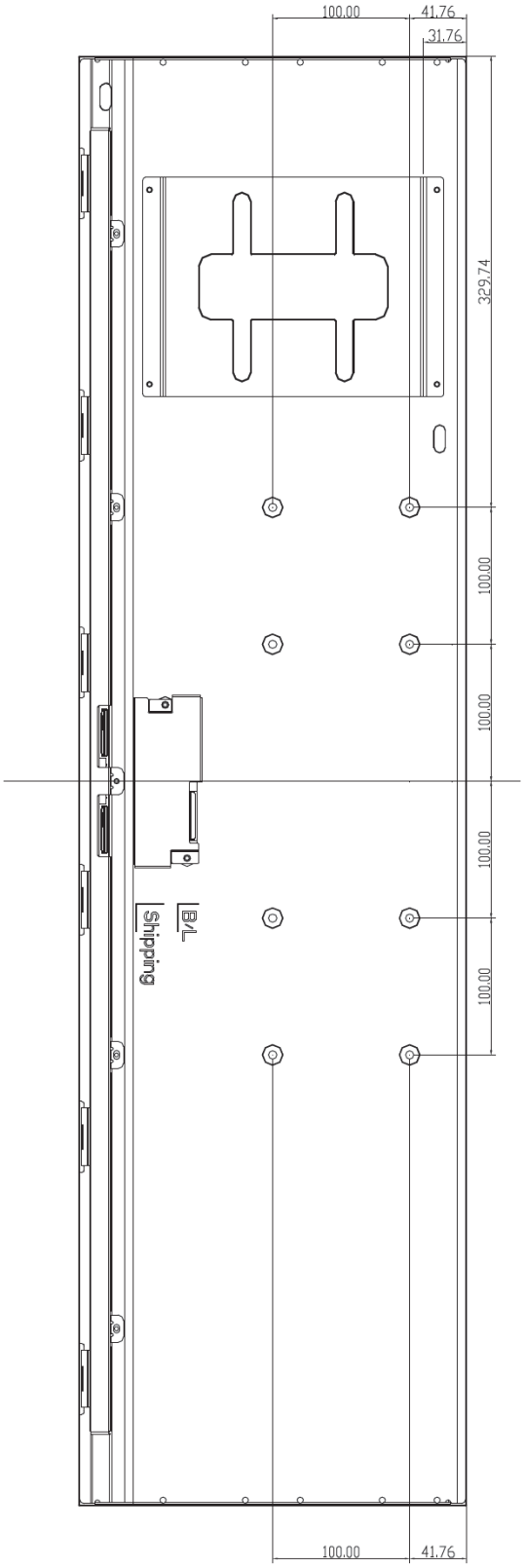
Note 1: The TFT-LCD module will not sustain damage after being subjected to 100 cycles of rapid temperature change. A cycle of rapid temperature change consists of varying the temperature from -20℃ to 60℃, and back again. Power is not applied during the test. After temperature cycling, the unit is placed in normal room ambient for at least 4 hours before power on.

Note 2: According to EN61000-4-2 , ESD class B: Some performance degradation allowed. No data lost. Self-recoverable. No hardware failures.

Note 3: The test items are tested by open frame type chassis.

6. Mechanical Characteristic (mm)

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41.76
31.76
329.74
100.00
100.00
100.00
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B/L
Shipping
100.00
41.76