58.4” 3840 x 1080

High brightness color TFT-LCD module

Model: VM59S1 V1

Version：01

Date: Jan. 27th, 2022

Note: This specification is subject to change without notice

Customer：_____ **Date：_____**

Approved	**Prepared**
Date:	**Date:**

Contents

RECORD OF REVISION

Version and Date	Page	Old description	New description	Remark
0.1 2022/01/27	All	First Edition for customer		

1. Handling Precautions

1) Since front polarizer is easily damaged, pay attention not to scratch it.
2) Be sure to turn off power supply when inserting or disconnecting from input connector.
3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
7) Do not open or modify the Module Assembly.
8) Do not press the reflector sheet at the back of the module to any directions.
9) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
10) After installation of the TFT Module into an enclosure, do not twist nor bend the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.

2. General Description

2.1 Overview

This specification applies to the Color Active Matrix Liquid Crystal Display composed of a TFT-LCD display a LED backlight system. The screen format is intended to support 3840(H) x1080(V)) screen and 1.07B (8 bits + FRC) color support.
LED driving board for backlight unit is included.

2.2 Features

- High brightness display, 1000nits by LED backlight.
- Long operation lifetime BLU design
- 4000:1 High contrast ratio
- Hi-Tni LC(-40~110C) applied
- Wide operation temperature
- RoHS Compliance

2.3 Application

Industrial applications.

2.4 Display specifications

Items	Unit	Specification
Screen Diagonal	inch	58.4”
Active Area	mm	1428.48 (H) X 401.76 (V)
Pixels H x V	pixels	3840 x3(RGB) x 1080
Pixels Pitch	um	372 (per one triad) x 372
Pixel Arrangement		RGB Vertical stripe
Display mode		Normally black
White luminance (center)	Cd/m^2	1000 (Typ)
Contrast ratio		4000:1 (Typ.)
Optical Response Time	msec	8 ms (Typ. On/off)
Normal Input Voltage VDD	Volt	12.0V
Power Consumption (Vcc Line + LED backlight)	Watt	166.2 W (VDD line=15.0 W; LED lines= 151.2 W)
Weight	Grams	TBD
Physical size	mm	1456.28 (W)× 429.56 (H)× 30.0 (D)
Electrical Interface		V by One
Support colors		1.07M colors (8 bits + FRC)
Surface Treatment		Hard coating
Temperature range Operating Storage	 ^0C ^0C	 -10 ~ 50 -20 ~ 60
RoHS Compliance		RoHS Compliance

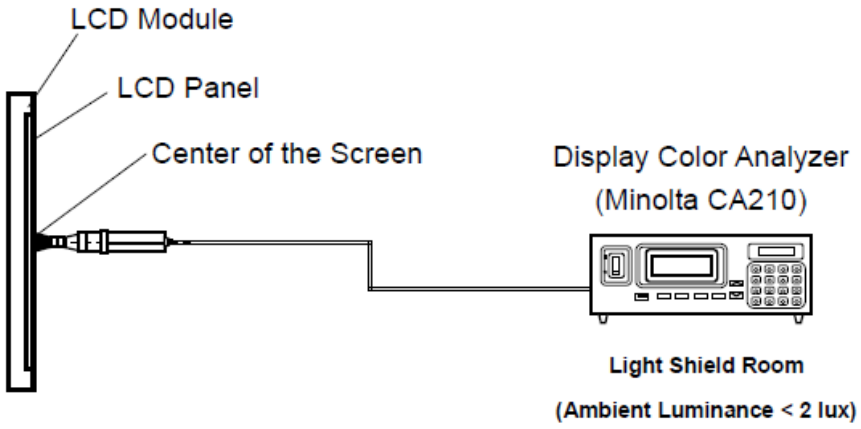
2.5 Optical characteristics

The following optical characteristics are measured under stable condition at 25 ^{0}C

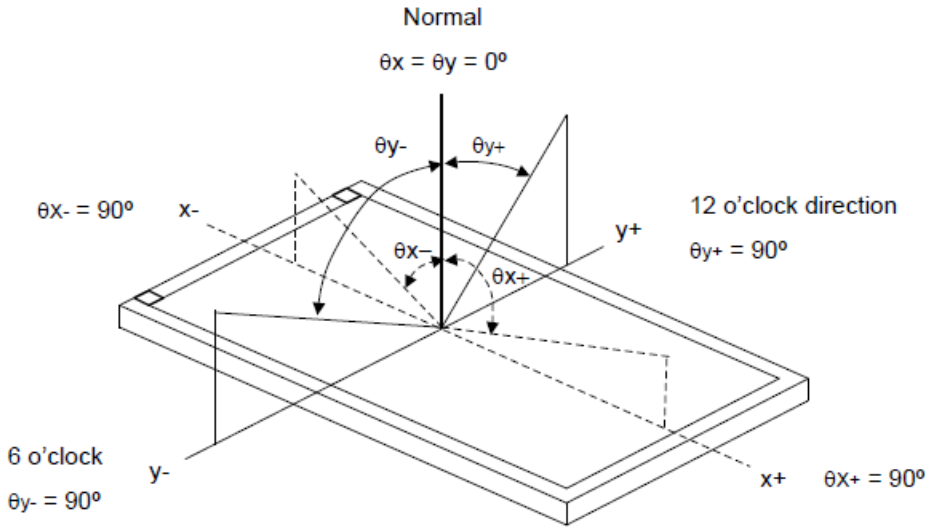
Items	Unit	Conditions	Min.	Typ.	Max.	Note
Viewing angle	Deg.	Horizontal (Right)	85	89		2
		CR=10 (Left)	85	89		
		Vertical (Up)	85	89		
		CR=10 (Down)	85	89		
Contrast Ratio		Normal Direction	3200	4000		3
Response Time	msec	Raising + Falling		8	16	4
Color coordinates (CIE) White		Red x	-0.05	0.650	+0.05	
		Red y		0.337		
		Green x		0.325		
		Green y		0.611		
		Blue x		0.153		
		Blue y		0.077		
		White x		0.313		5
		White y		0.329		
Center Luminance	Cd/m^2		800	1000		6
Luminance Uniformity	%		70	75		7
NTSC	%			72		
Crosstalk (in 60 Hz)	%				1.5	
Flicker	dB				-20	

Note 1: Measurement method

The LCD module should be stabilized at given temperature for 0.5 hour to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 1 hour in a windless room.



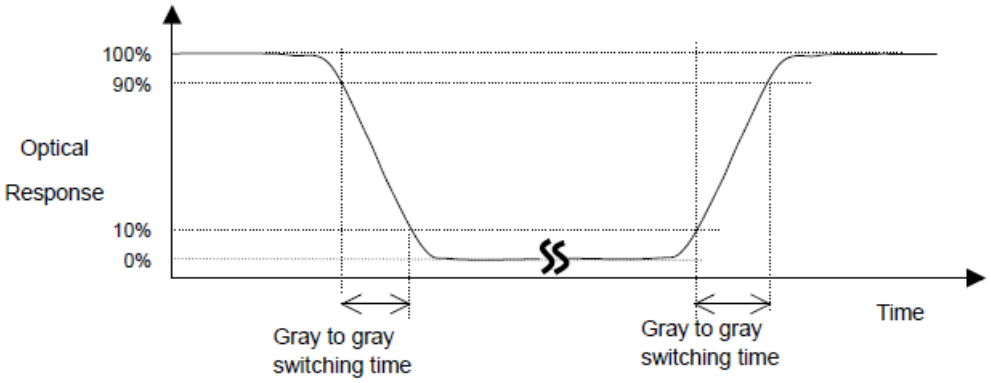
Note 2: Definition of viewing angle



Note 3: Contrast ratio is measured by Minolta CA210

Note 4: Definition of Response time

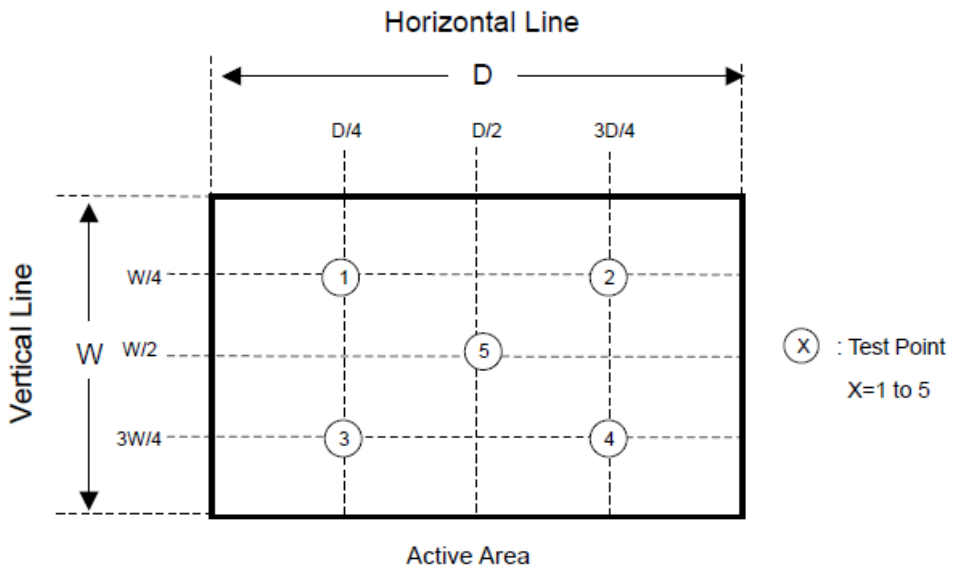
The output signals of photo detector are measured when the input signals are changed from “Full Black” to “Full White” (rising time), and from “Full White” to “Full Black” (falling time), respectively. The response time is interval between the 10% and 90% of amplitudes. Please refer to the figure as below.



Note 5: Color chromaticity and coordinates (CIE) is measured by Minolta CA210

Note 6: Center luminance is measured by Minolta CA210

Note 7: Luminance uniformity of these 5 points is defined as below and measured by Minolta CA210



Uniformity = (Min. Luminance of 5 points) / (Max. Luminance of 5 points)

3. Absolute Maximum Ratings

Absolute maximum ratings of the module are as following:

3.1 TFT LCD module

Items	Symbol	Min	Max	Unit	Conditions
Power supply voltage	V_{DD}	-0.3	14	Volt	Note 1, 2
Input voltage of signal	Vin	-0.3	4	Volt	Note 1, 2

3.2 Backlight unit

Items	Symbol	Min	Max	Unit	Conditions
LED bar input voltage			26.4	V	

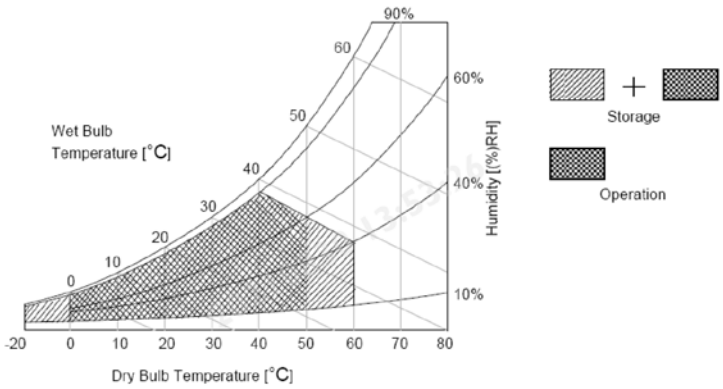
3.3 Environment

Items	Symbol	Values			Unit	Conditions
		Min.	Typ.	Max.		
Operation temperature	T_{OS}	-10	-	50	^{0}C	Note 3
Operation Humidity	H_{OP}	10		85	%	
Storage temperature	T_{ST}	-20		60	^{0}C	
Storage Humidity	H_{ST}	5		90	%	

Note 1: With in Ta= 25℃

Note 2: Permanent damage to the device may occur if exceed maximum values

Note 3: For quality performance, please refer to IIS (Incoming Inspection Standard).



4. Electrical characteristics

4.1 LCD electronics specification

4.1.1 Power specification

Item		Symbol	Min.	Typ.	Max	Unit	Note
Power Supply Input Voltage		V_{DD}	10.8	12	13.2	V	1
Power Supply Input Current	Black pattern	I_{DD}	-	0.92	1.10	A	2
	White pattern		-	1.25	1.50	A	
	H-strip pattern		-	1.21	1.45	A	
Power Consumption	Black pattern	P_C	-	11.04	14.52	Watt	
	White pattern		-	15.00	19.80	Watt	
	H-strip pattern		-	14.52	19.14	Watt	
Inrush Current		I_{RUSH}	--	--	5	A	3

Note1. The ripple voltage should be fewer than 5% of VDD.

Note2. Test Condition:

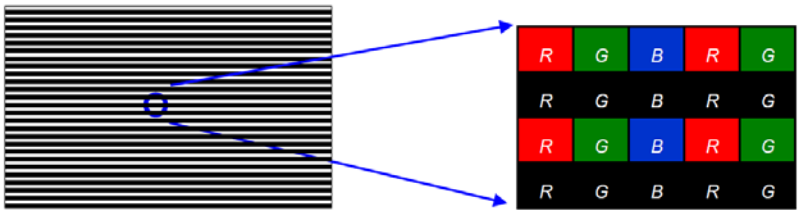
(1) V_{DD} = 12.0V, (2) Fv = 60Hz, (3) Fclk= 74.25MHz, (4) Temperature = 25 ℃

(5) Power dissipation check pattern. (Only for power design)

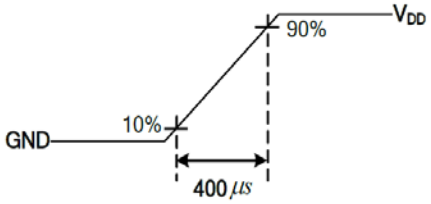
a. Black pattern

b. White pattern

c. H-Strip pattern



Note3. Measurement condition: Rising time = 400us



4.2 Backlight unit

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks (Test Condition)
Input Specification						
Input Voltage	**V_{in}**	21.6	24.0	26.4	V_{DC}	Input voltage: 24 V_{DC}
Input Current	**I_{in}**		6.3		A_{DC}	
BLU power	**P_{BLU}**		151.2		W	
On/Off control	**ON/OFF**	3.3	-	5.0	V_{DC}	ON STATE
		-	0	0.8		OFF STATE
Dimming (Analog)	**DIM**		3.3	5.0	V_{DC}	Min. Brightness
			0			Max. Brightness
Dimming (PWM)	**DIM**	-	3.3	5.0	V_{DC}	High level
		-	0	-		Low level
		10		100	%	Dimming range
		200	300	500	Hz	Dimming frequency
BLU lifetime	**MTBF**		50,000		hr	

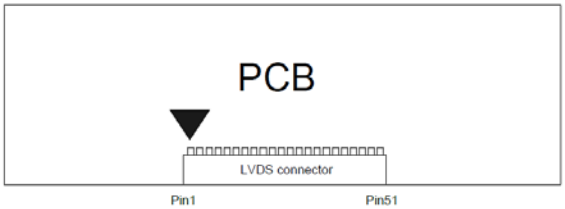
4.3 Interface connector

4.3.1 TFT connector(CN1)

■ LCD connector: (JAE) SJ11346-FI-RTE51SZ-HF, (P2)187059-51221-1,(Starconn)115E51-0000RA-M3-R

PIN	Symbol	Description	Note	PIN	Symbol	Description	Note
1	V_{DD}	12Vin		26	LOCKN	Vx1 LOCK	
2	V_{DD}	12Vin		27	GND	Ground	
3	V_{DD}	12Vin		28	RX0N	Vx1 lane 0	
4	V_{DD}	12Vin		29	RX0P	Vx1 lane 0	
5	V_{DD}	12Vin		30	GND	Ground	
6	V_{DD}	12Vin		31	RX1N	Vx1 lane 1	
7	V_{DD}	12Vin		32	Rx1P	Vx1 lane 1	
8	V_{DD}	12Vin		33	GND	Ground	
9	N.C.	No connection	2	34	RX2N	Vx1 lane 2	
10	GND	Ground		35	RX2P	Vx1 lane2	
11	GND	Ground		36	GND	Ground	
12	GND	Ground		37	RX3N	Vx1 lane 3	
13	GND	Ground		38	RX3P	Vx1 lane 3	
14	GND	Ground		39	GND	Ground	
15	N.C.	No connection		40	RX4N	Vx1 lane 4	
16	N.C.	No connection		41	RX4P	Vx1 lane 4	
17	N.C.	No connection	2	42	GND	Ground	
18	N.C.	No connection	2	43	RX5N	Vx1 lane 5	
19	N.C.	No connection	2	44	RX5P	Vx1 lane 5	
20	N.C.	No connection	2	45	GND	Ground	
21	N.C.	No connection	2	46	RX6N	Vx1 lane 6	
22	N.C.	No connection	2	47	RX6P	Vx1 lane 6	
23	N.C.	No connection	2	48	GND	Ground	
24	GND	Ground		49	RX7N	Vx1 lane 7	
25	HTPDN	Vx1 HTPDN		50	RX7P	Vx1 lane 7	
				51	GND	Ground	

Note1. Pin number start from the left side as the following figure.



Note2. Please leave this pin unoccupied. It cannot be connected with any signal (Low/GND/High).

4.3.2 Backlight connector(CN2)

Connector: CviLux CI0114M1HR0 or equivalent

Pin NO	Symbol	Description
1	VIN	DC +24V
2	VIN	DC +24V
3	VIN	DC +24V
4	VIN	DC +24V
5	VIN	DC +24V
6	GND	Ground
7	GND	Ground
8	GND	Ground
9	GND	Ground
10	GND	Ground
11	NC	No connected
12	ON / OFF	OFF=0V; ON=+5V
13	DIMM	20~100%
14	NC	No connected

5. Signal characteristics

5.1 B by one color data mapping

Mode	Packer input & Unpacker output		30bpp RGB / YCbCr444 (10bit)
4byte mode	Byte0	D[0]	R/Cr[2]
		D[1]	R/Cr[3]
		D[2]	R/Cr[4]
		D[3]	R/Cr[5]
		D[4]	R/Cr[6]
		D[5]	R/Cr[7]
		D[6]	R/Cr[8]
		D[7]	R/Cr[9]
	Byte1	D[8]	G/Y[2]
		D[9]	G/Y[3]
		D[10]	G/Y[4]
		D[11]	G/Y[5]
		D[12]	G/Y[6]
		D[13]	G/Y[7]
		D[14]	G/Y[8]
		D[15]	G/Y[9]
	Byte2	D[16]	B/Cb[2]
		D[17]	B/Cb[3]
		D[18]	B/Cb[4]
		D[19]	B/Cb[5]
		D[20]	B/Cb[6]
		D[21]	B/Cb[7]
		D[22]	B/Cb[8]
		D[23]	B/Cb[9]
	Byte3	D[24]	--
		D[25]	--
		D[26]	B/Cb[0]
		D[27]	B/Cb[1]
		D[28]	G/Y[0]
		D[29]	G/Y[1]
		D[30]	R/Cr[0]
		D[31]	R/Cr[1]

5.2 Color input data reference

The brightness of each primary color (red, green and blue) is based on the 10 bit gray scale data input for the color; the higher the binary input, the brighter the color. The table below provides a reference for color versus data input.

COLOR DATA REFERENCE

Color		Input Color Data																													
		RED										GREEN										BLUE									
		MSB									LSB	MSB									LSB	MSB									LSB
		R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	G9	G8	G7	G6	G5	G4	G3	G2	G1	G0	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Basic Color	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(1023)	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(1023)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	Blue(1023)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R	RED(000)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED(001)	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	RED(1022)	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED(1023)	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
G	GREEN(000)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	GREEN(001)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0

	GREEN(1022)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0
	GREEN(1023)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
B	BLUE(000)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	BLUE(001)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

	BLUE(1022)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0
	BLUE(1023)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1

6. Signal timing specification

6.1 Input timing

6.1.1 Timing table

Timing Table (DE only Mode)

Signal	Item	Symbol	Min.	Typ.	Max	Unit
Vertical Section	Period	Tv	2200	2250	2715	Th
	Active	Tdisp (v)		2160		
	Blanking	Tblk (v)	40	90	555	Th
Horizontal Section	Period	Th	530	550	600	Tclk
	Active	Tdisp (h)		480		
	Blanking	Tblk (h)	50	70	120	Tclk
Clock	Frequency	Fclk=1/Tclk	66	74.25	77	MHz
Vertical Frequency	Frequency	Fv	47	60	63	Hz
Horizontal Frequency	Frequency	Fh	120	135	139.2	KHz

Notes:

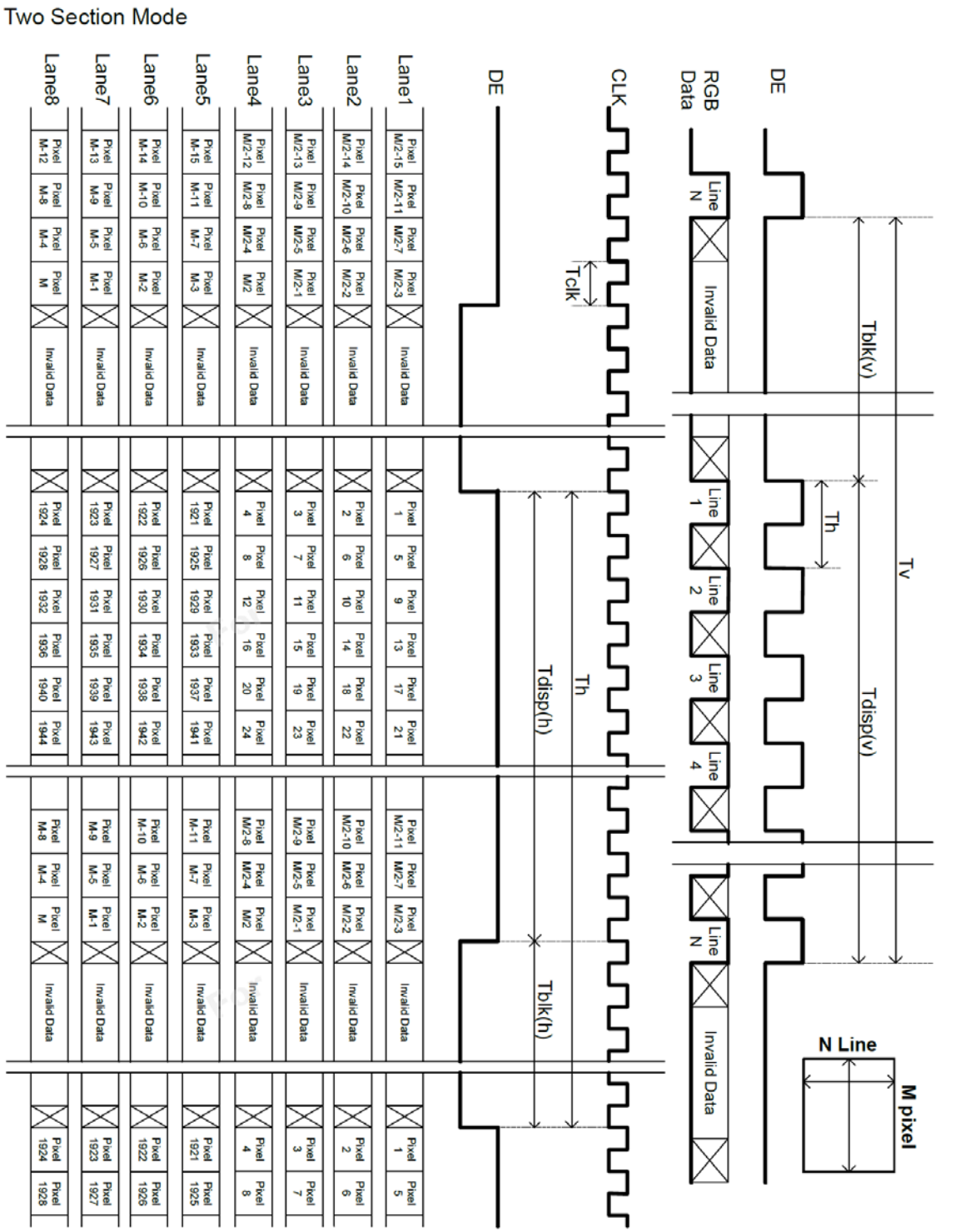
(1) Display position is specific by the rise of DE signal only.
Horizontal display position is specified by the rising edge of 1st DCLK after the rise of 1st DE, is displayed on the left edge of the screen.

(2) Vertical display position is specified by the rise of DE after a "Low" level period equivalent to eight times of horizontal period. The 1st data corresponding to one horizontal line after the rise of 1st DE is displayed at the top line of screen.

(3) If a period of DE "High" is less than 3840 DCLK or less than 2160 lines, the rest of the screen displays black.

(4) The display position does not fit to the screen if a period of DE "High" and the effective data period do not synchronize with each other.

6.1.2 Signal timing waveform



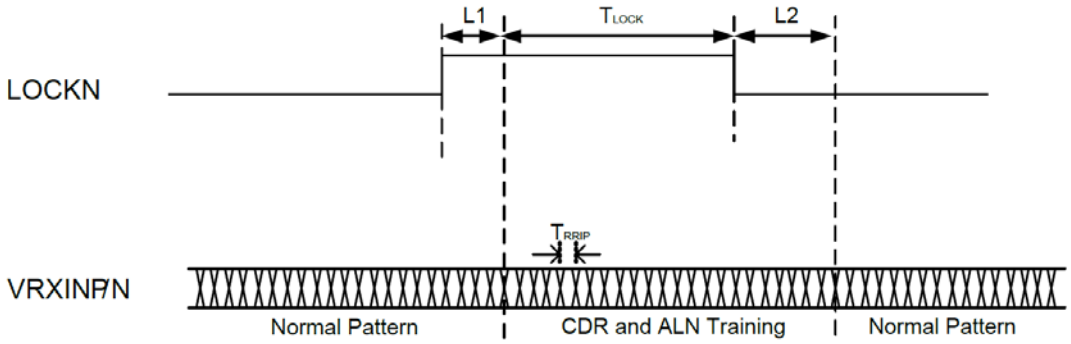
6.2 Input interface characteristics

V by One spec

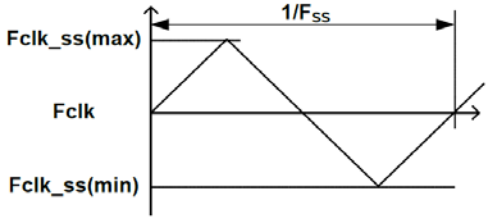
Item		Symbol	Min.	Typ.	Max	Unit	Note
V-by-one Interface	VRXINP/N input each bit Period	T_{RRIP} (UI)	310	--	379	ps	10bit 1
	Receiver Clock: Spread Spectrum Modulation range	Fclk_ss	Fclk -0.5%	--	Fclk +0.5%	MHz	2
	Receiver Clock: Spread Spectrum Modulation frequency	Fss		30		KHz	2
	CDR training pattern time	T_{LOCK}	--	500	--	us	1
	Latency from LOCKN 'HIGH' to clock training pattern	L1	0	--	--	us	1
	Latency from LOCKN 'LOW' to normal 8b10b data	L2	--	--	70	us	1
	CML Differential Input High Threshold	V_{RTH}	--	--	+50	mV_{DC}	
	CML Differential Input Low Threshold	V_{RTL}	-50	--	--	mV_{DC}	
	CML Common mode Bias Voltage	V_{RCT}	0.8	0.9	1.0	Vdc	
	Intra-pair skew	T_{INTRA}	--	--	0.3	UI	3
	Inter-pair skew	T_{INTER}	--	--	5	UI	4
	Eye diagram at receiver	A_X	--	0.25	--	UI	5
		A_Y	--	0	--	mV	
		B_X	--	0.3	--	UI	
		B_Y	--	50	--	mV	
		C_X	--	0.7	--	UI	
		C_Y	--	50	--	mV	
		D_X	--	0.75	--	UI	
		D_Y	--	0	--	mV	
		E_X	--	0.7	--	UI	
		E_Y	--	-50	--	mV	
		F_X	--	0.3	--	UI	
		F_Y	--	-50	--	mV	

Note:

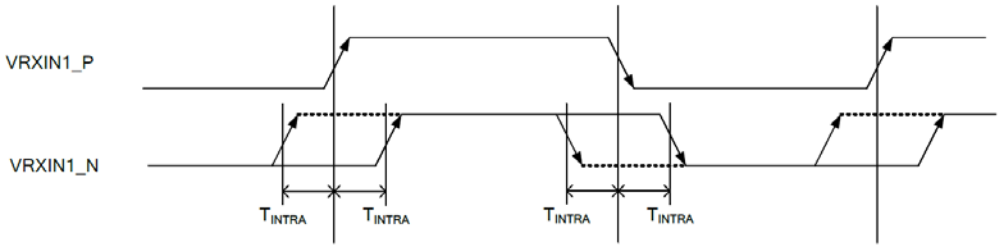
1. V-by-one Signal diagram



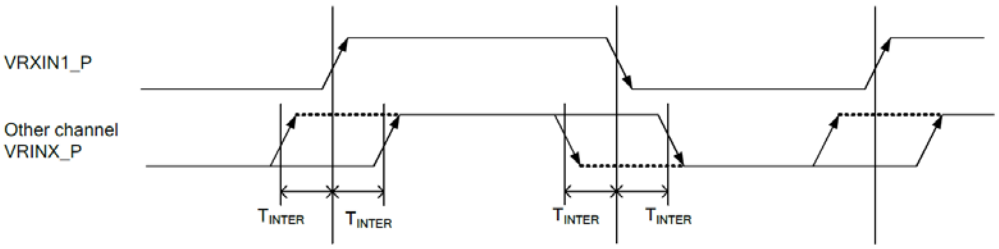
2. Receiver Clock SSCG (Spread spectrum clock generator) is defined as below figures.



3. V-by-one Intra-pair Skew

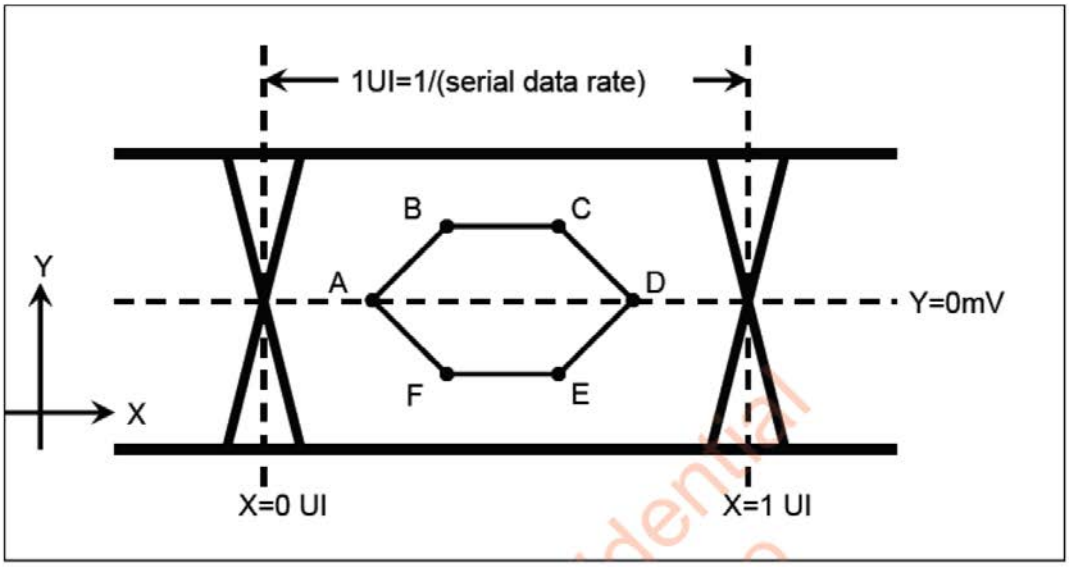


4. V-by-one Inter-pair Skew



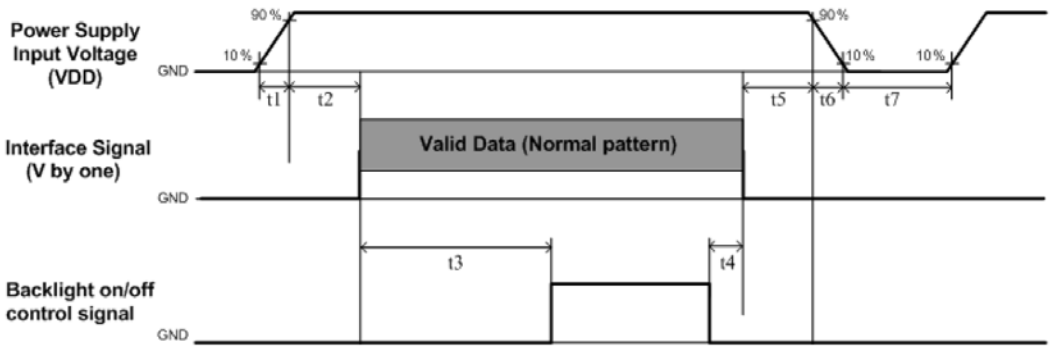
5. Eye diagram at receiver

Eye Mask



Example of Eye diagram

6.3 Power sequence for LCD



Parameter	Values			Unit
	Min.	Type.	Max.	
t1	0.4	---	30	ms
t2	40	---	---	ms
t3	640	---	---	ms
t4	0*1	---	---	ms
t5	0	---	---	ms
t6	---	---	---*2	ms
t7	1000*3	---	---	ms

Note :

(1) t4=0 : concern for residual pattern before BLU turn off.

(2) t6 : voltage of VDD must decay smoothly after power-off. (customer system decide this value)

(3) When the power supply input voltage(VDD) is off, be sure to pull down the valid and the invalid data to 0V.

7. Reliability Test

Environment test conditions are listed as following table.

Items	Required Condition	Note
Temperature Humidity Bias (THB)	Ta=40℃, 80%RH, 120hours	
High Temperature Operation (HTO)	Ts= 50℃, 120hours	
Low Temperature Operation (LTO)	Ta= -10℃, 120hours	
High Temperature Storage (HTS)	Ta= 60℃, 120hours	
Low Temperature Storage (LTS)	Ta= -20℃, 120hours	
Thermal Shock Test (TST)	-20℃/30min, 60℃/30min, 100 cycles	
ESD (ElectroStatic Discharge)	Contact Discharge: ± 8KV, 150pF(330Ω) 1sec, 9 points, 25 times/ point.	
	Air Discharge: ± 15KV, 150pF(330Ω) 1sec 9 points, 25 times/ point.	

Note 1: The TFT-LCD module will not sustain damage after being subjected to 100 cycles of rapid temperature change. A cycle of rapid temperature change consists of varying the temperature from -10℃ to 50℃, and back again. Power is not applied during the test. After temperature cycling, the unit is placed in normal room ambient for at least 4 hours before power on.

Note 2: According to EN61000-4-2 , ESD class B: Some performance degradation allowed. No data lost. Self-recoverable. No hardware failures.

Note 3: TFT surface.

8. Shipping package
(TBD)

9. Mechanical Characteristics