5.0” 720 x 1280

High brightness color TFT-LCD module

Model: VM05B4 VN

Date: Jul. 16th, 2021

Version：01

Note: This specification is subject to change without notice

Customer：_____ **Date：_____**

Approved	**Prepared**
Date:	**Date:**

Contents

RECORD OF REVISION

Version and Date	Page	Old description	New description	Remark
0.1 2021/07/16	All	First Edition for customer		

1. Handling Precautions

1) Since front polarizer is easily damaged, pay attention not to scratch it.
2) Be sure to turn off power supply when inserting or disconnecting from input connector.
3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
7) Do not open or modify the Module Assembly.
8) Do not press the reflector sheet at the back of the module to any directions.
9) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
10) After installation of the TFT Module into an enclosure, do not twist nor bend the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.

2. General Description

2.1 Overview

This specification applies to the Color Active Matrix Liquid Crystal Display composed of a TFT-LCD display a LED backlight system. The screen format is intended to support 720(H) x 1280(V) screen.

2.2 Features

- High brightness display by LED backlight.
- Long operation lifetime BLU design
- mipi interface
- Wide view angle
- Wide operation temperature
- RoHS Compliance

2.3 Application

Industrial applications.

2.4 Display specifications

Items	Unit	Specification
Screen Diagonal	inch	4.98”
Active Area	mm	62.1 (H) X 110.4 (V)
Pixels H x V	pixels	720 x3(RGB) x 1280
Pixels Pitch	um	86.25 (per one triad) x 86.25
Pixel Arrangement		RGB Vertical stripe
Display mode		Normally black
White luminance (center)	Cd/m^2	480 (Typ)
Contrast ratio		800:1 (Typ.)
Optical Response Time	msec	20 ms (Typ. On/off)
Normal Input Voltage VDD	Volt	2.8
Power Consumption (Vcc Line + LED backlight)	Watt	TBD (VDD line=TBD; LED lines= 0.896 W)
Weight	Grams	TBD
Physical size	mm	65.3 (W)× 119.3 (H)× 1.73 (D, w PCB)
Electrical Interface		MIPI (2Lane)
Driver IC		ILI9881D
Temperature range Operating Storage	 ^0C ^0C	 -20 ~ 70 (TFT surface) -30 ~ 80
RoHS Compliance		RoHS Compliance

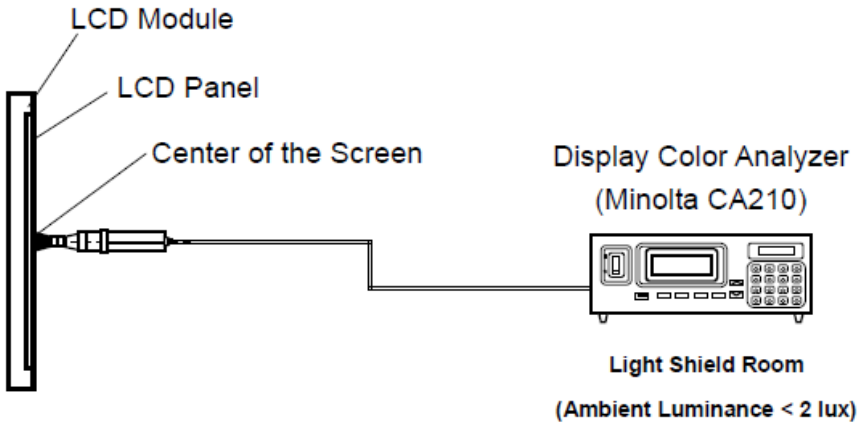
2.5 Optical characteristics

The following optical characteristics are measured under stable condition at 25 ^{0}C

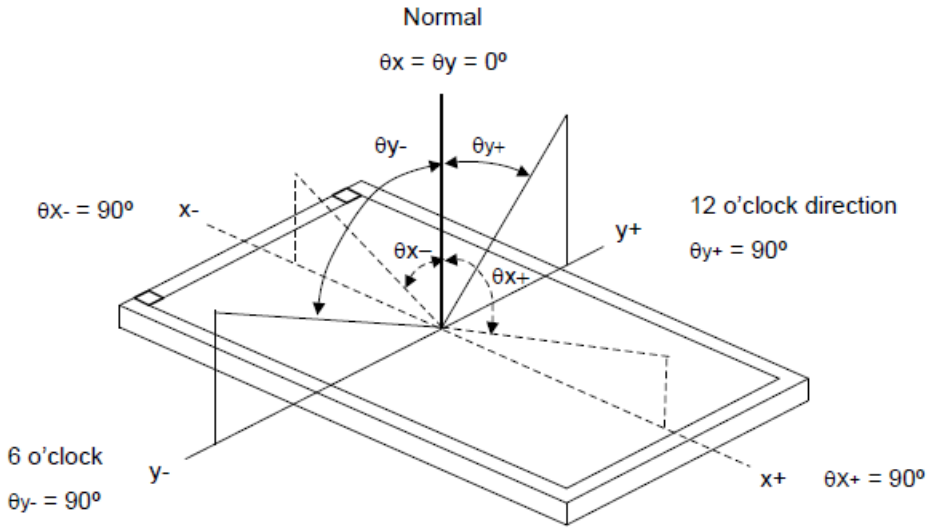
Items	Unit	Conditions	Min.	Typ.	Max.	Note
Viewing angle	Deg.	Horizontal (Right) CR=10 (Left)		80 80		2
		Vertical (Up) CR=10 (Down)		80 80		
Contrast Ratio		Normal Direction	640	800		3
Response Time	msec	Raising + Falling		20	25	4
Color / Chromaticity Coordinates (CIE)		Red x	-0.05	0.654	+0.05	5
		Red y		0.319		
		Green x		0.259		
		Green y		0.574		
		Blue x		0.140		
		Blue y		0.084		
Color coordinates (CIE) White		White x		0.310		
		White y		0.329		
Center Luminance	Cd/m^2			480		6
Luminance Uniformity	%		70	75		7
Crosstalk (in 60 Hz)	%				1.5	
Flicker	dB				-20	

Note 1: Measurement method

The LCD module should be stabilized at given temperature for 0.5 hour to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 1 hour in a windless room.



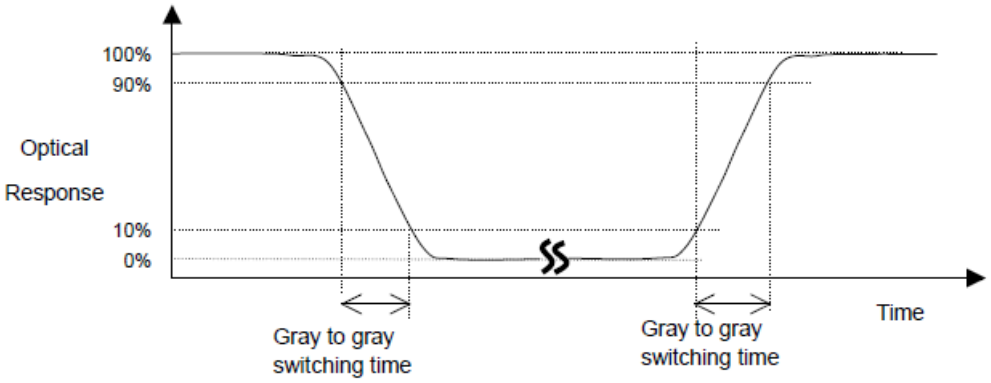
Note 2: Definition of viewing angle



Note 3: Contrast ratio is measured by Minolta CA210

Note 4: Definition of Response time

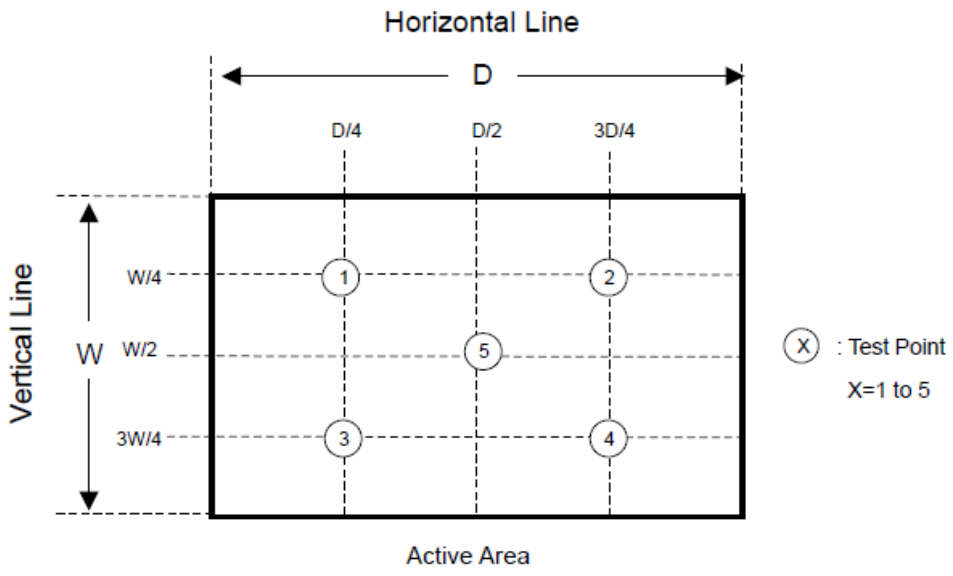
The output signals of photo detector are measured when the input signals are changed from “Full Black” to “Full White” (rising time), and from “Full White” to “Full Black” (falling time), respectively. The response time is interval between the 10% and 90% of amplitudes. Please refer to the figure as below.



Note 5: Color chromaticity and coordinates (CIE) is measured by Minolta CA210

Note 6: Center luminance is measured by Minolta CA210

Note 7: Luminance uniformity of these 5 points is defined as below and measured by Minolta CA210



Uniformity = (Min. Luminance of 5 points) / (Max. Luminance of 5 points)

3. Absolute Maximum Ratings

Absolute maximum ratings of the module are as following:

3.1 TFT LCD module

Items	Symbol	Min	Max	Unit	Conditions
Power supply voltage 1	V_{CC}	-0.3	6.5	Volt	Note 1, 2
Power supply voltage 2	IOV_{CC}	-0.3	5.5	Volt	

3.2 Backlight unit

Items	Symbol	Min	Max	Unit	Conditions
LED bar input current			50	mA	

3.3 Environment

Items	Symbol	Values			Unit	Conditions
		Min.	Typ.	Max.		
Operation temperature	T_{OS}	-20	-	70	^{0}C	Note 3
Operation Humidity	H_{OP}	10		85	%	
Storage temperature	T_{ST}	-30		80	^{0}C	
Storage Humidity	H_{ST}	5		90	%	

Note 1: With in Ta= 25℃

Note 2: Permanent damage to the device may occur if exceed maximum values

Note 3: For quality performance, please refer to IIS (Incoming Inspection Standard).

4. Electrical characteristics

4.1 LCD electronics specification

AGND = GND = 0V, Ta = 25℃

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage for analog circuit	VCC	2.5	2.8	3.3	V
Supply voltage for logic circuit	IOVCC	1.65	1.8	2.0	V
Input voltage 'H'level	V_{IH}	0.7*IOVCC	—	IOVCC	V
Input voltage 'L'level	V_{IL}	GND	—	0.3*IOVCC	V
Output voltage 'H'level	V_{OH}	0.8*IOVCC	—	IOVCC	V
Output voltage 'L'level	V_{OL}	GND	—	0.2*IOVCC	V

4.2 Backlight unit

Parameter	Min	Typ	Max	Unit	Note
LED voltage (VL)		22.4		[V]	2
LED current (IL)		40		[mA]	2
LED power (PL)		0.896		[W]	
LED lite time (MTBF)	20,000			[Hour]	1

Note 1: The “LED lift time” is defined as the module brightness decrease to 50% original brightness that the ambient temperature is 25℃ and typical LED Current at 40 mA

Note 2: The variance of LED Light Bar power consumption is ±10%. Calculator value for reference (IL × VL = PLED)

4.3 Interface connector

4.3.1 TFT connector(CN1)

Pin No.	Symbol	Description
1	GND	Power ground
2	TOUCH_3V3	CTP-Power supply
3	GND	Power ground
4	TOUCH_INT	CTP-INT
5	TOUCH_RST	CTP-Reset signal
6	TOUCH_SDA	CTP-SDA
7	TOUCH_SCL	CTP-SCL
8	GND	Power ground
9	LEDK	LED backlight cathode
10	LEDA	LED backlight anode
11	ID	LCM-ID signal
12	RSTN	Reset signal(low active)
13	NC	NC
14	IOVCC3V3	Power supply for the logic power and I/O circuit
15	VCC3V3	Power supply for the analog power
16	GND	Power ground
17	NC	NC
18	NC	NC
19	GND	Power ground
20	NC	NC
21	NC	NC
22	GND	Power ground
23	CKP	MIPI-DSI clock posivtve input pin
24	CKN	MIPI-DSI clock negtive input pin
25	GND	Power ground
26	D1P	MIPI-DSI data lane 1 posivtve input pin
27	D1N	MIPI-DSI data lane 1 negtive input pin
28	GND	Power ground
29	D0P	MIPI-DSI data lane 0 posivtve input pin
30	D0N	MIPI-DSI data lane 0 negtive input pin
31	GND	Power ground

5. Signal characteristics

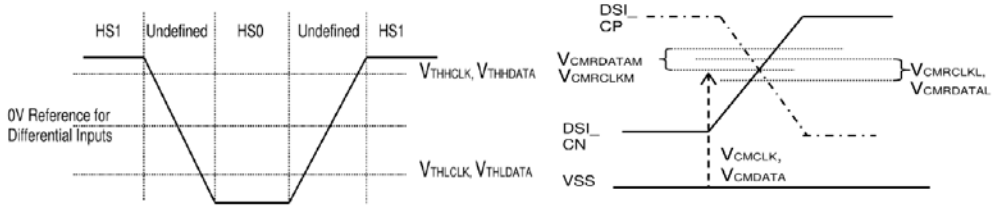
5.1 LP mode

Parameter	Symbol	Conditions	Spec.			Unit
			Min.	Typ.	Max.	
Logic high level input voltage	V_{IHLPCD}	LP-CD	450	-	1350	mV
Logic low level input voltage	V_{ILLPCD}	LP-CD	0	-	200	mV
Logic high level input voltage	V_{IHLPRX}	LP-RX(CLK, D0)	880	-	1350	mV
Logic low level input voltage	V_{ILLPRX}	LP-RX(CLK, D0)	0	-	550	mV
Logic low level input voltage	$V_{ILLPRXULP}$	LP-RX(CLK ULP mode)	0	-	300	mV
Logic high level output voltage	V_{OHLPTX}	LP-TX(D0)	1.1	-	1.3	V
Logic low level output voltage	V_{OLLPTX}	LP-TX(D0)	-50	-	50	mV
Logic high level input current	V_{IH}	LP-CD, LP-RX	-	-	10	uA
Logic low level input current	V_{IL}	LP-CD, LP-RX	-10	-	-	uA
Input pulse rejection	SGD	DSI-CLK+/-, DSI-D0+/1	-	-	300	Vps

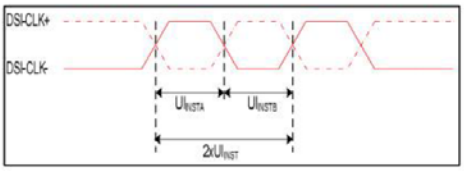
Input glitch rejections of low-power receivers

5.2 High speed mode

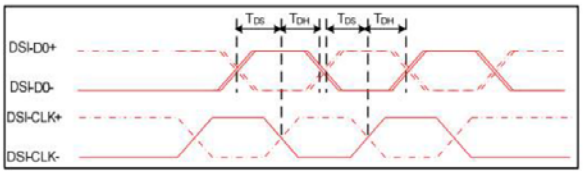
Parameter	Symbol	Conditions	Spec.			Unit
			Min.	Typ.	Max.	
Input common mode	V_{CMCLK} V_{CMDATA}	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	70	-	330	mV
Input common mode variation <450 MHZ	$V_{CMRCLKL}$ $V_{CMRDATAL}$	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	-50	-	50	mV
Input common mode variation >450 MHZ	$V_{CMRCLKM}$ $V_{CMRDATAM}$	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	-	-	100	mV
Low-level differential Input threshold	V_{THLCLK} $V_{THLDATA}$	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	-70	-	-	mV
High-level differential Input threshold	V_{THHCLK} $V_{THHDATA}$	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	-	-	70	mV
Single ended input low voltage	V_{ILHS}	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	-40	-	-	mV
Single ended input high voltage	V_{IHHS}	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	-	-	460	mV
Differential input termination resistor	R_{TERM}	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	80	100	125	Ω
Single-ended threshold voltage for termination enable	V_{TERMEN}	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	-	-	450	mV
Termination capacitor	C_{TERM}	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	-	-	-	pF



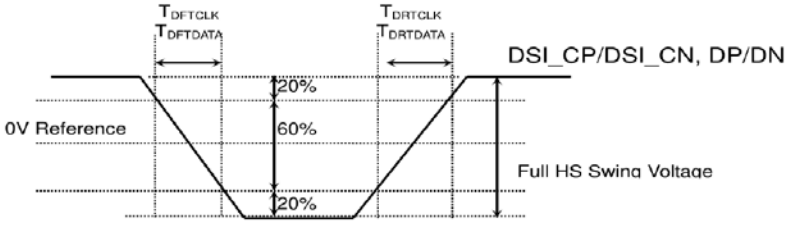
Differential voltage range and Command mode voltage



DSI clock channel timing



Rising and falling time on clock and data channel



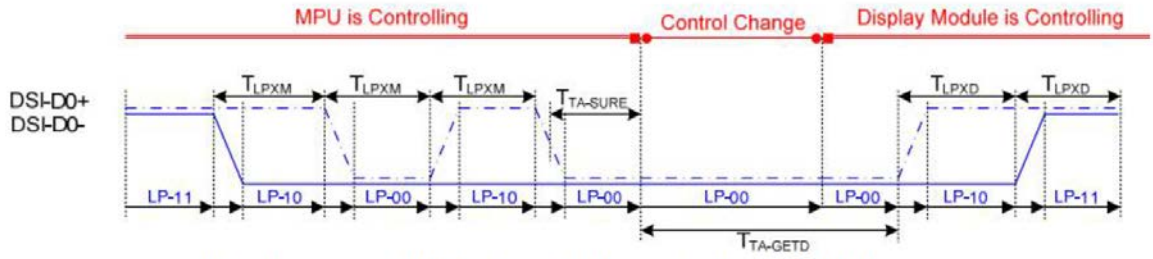
Rising and falling time on clock and data channel

(VSSA=0V, IOVCC=1.65V to 3.3V, VCI=2.5V to 3.3V, T_A = -30 to 70°C)

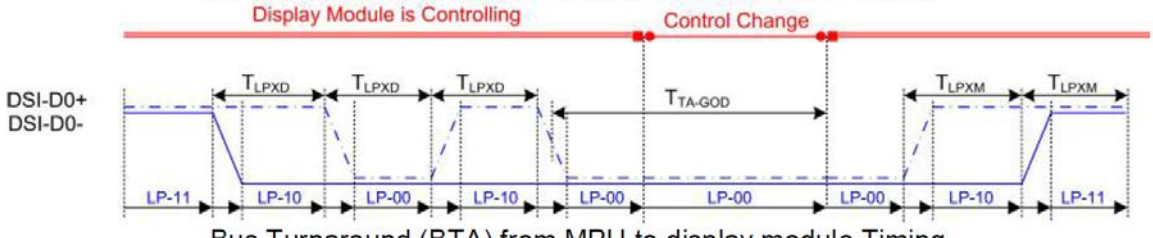
Signal	Item	Symbol	Spec.			Unit
			Min.	Typ.	Max.	
DSI_CP/ DSI_CN	Double UI instantaneous	2xUINST	TBD	-	25	ns
	UI instantaneous	UINSTA UINSTB	TBD	-	12.5	ns
DP/DN	Data to clock setup time	TDS	0.15xUI	-	-	ps
	Data to clock hold time	TDH	0.15xUI	-	-	ps
DSI_CP/ DSI_CN	Differential rise time for clock	TDRTCLK	150	-	0.3UI	ps
	Differential fall time for clock	TDFTCLK	150	-	0.3UI	ps
DP/DN	Differential rise time for data	TDRTDATA	150	-	0.3UI	ps
	Differential fall time for data	TDFTDATA	150	-	0.3UI	ps

High Speed Mode Timing Characteristics

5.3 Low power mode



Bus Turnaround (BTA) from display module to MPU Timing



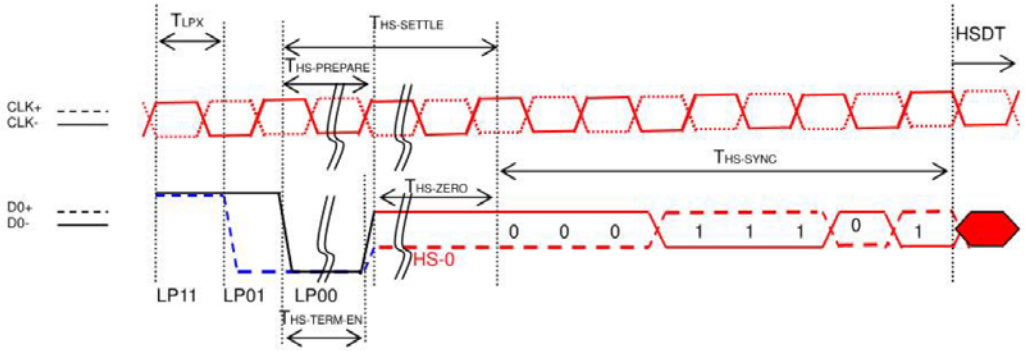
Bus Turnaround (BTA) from MPU to display module Timing

(VSSA=0V, IOVCC=1.65V to 2.0V, VCI=2.3V to 3.3V, T_A = -30 to 70°C)

Signal	Item	Symbol	Spec.			Unit
			Min.	Typ.	Max.	
DSI_D0P/ DSI_D0P	Length of LP-00/LP01/LP10/LP11 Host→ Display module	T_{LPXM}	50	-	-	ns
	Length of LP-00/LP01/LP10/LP11 Display module →Host	T_{LPXD}	50	-	-	ns
	Time-out before the MPU start driver	$T_{TA-SURE}$	T_{LPXD}	-	2xT_{LPXD}	ns
	Time to drive LP-00 by display module	T_{TA-GET}	5xT_{LPXD}	-	-	ns
	Time to drive LP-00 after turnaround request Host	T_{TAGO}	4xT_{LPXD}	-	-	ns

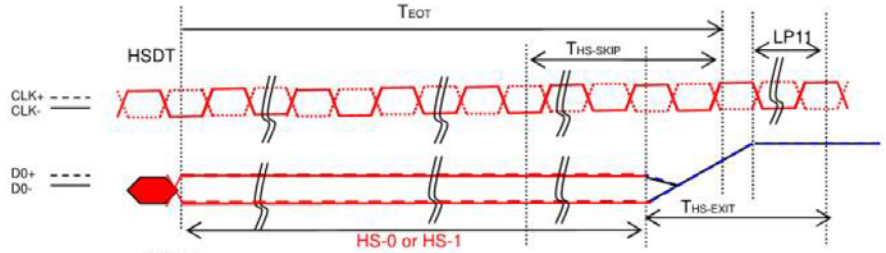
DSI Low Power Mode Characteristics

5.4 DSI bursts mode



Signal	Item	Symbol	Spec.			Unit
			Min.	Typ.	Max.	
DSI_D0P/ DSI_D0P	Length of LP-00/LP01/LP10/LP11	T_{LPX}	50	-	-	ns
	Time to Driver LP-00 to prepare for HS transmission	$T_{HS-PREPARE}$	40+4UI	-	85+6UI	ns
	Time to enable data receiver line termination	$T_{HS-TERM-EN}$	-	-	35+4xUI	ns
	Time to drive LP-00 by display module	T_{TA-GET}	5xT_{LPXD}	-	-	ns
	Time to drive LP-00 after turnaround request Host	T_{TAGO}	4xT_{LPXD}	-	-	ns

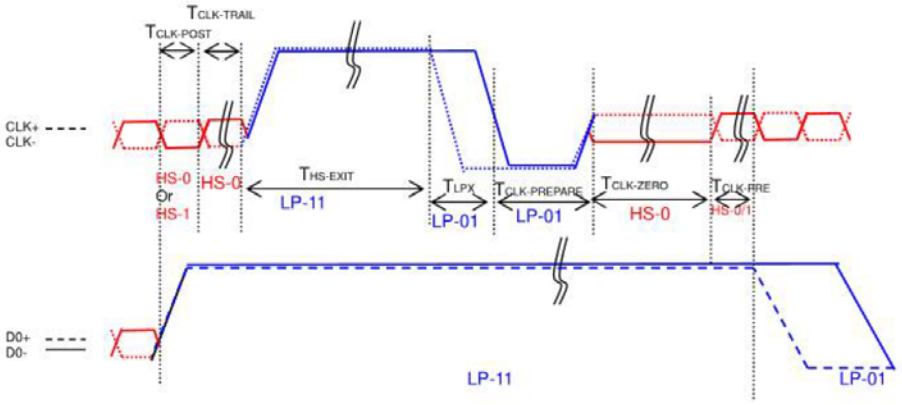
DSI Low Power Mode to/from High Speed Mode Timing



NOTE:
If the last bit is HS-0, the transmitter changes from HS-0 to HS-1
If the last bit is HS-0, the transmitter changes from HS-1 to HS-0

Signal	Item	Symbol	Spec.			Unit
			Min.	Typ.	Max.	
DSI_D0P/ DSI_D0P	Time-Out at Display Module to Ignore Transition Period of EoT	$T_{HS-SKIP}$	40	-	55+4xUI	ns
	Time to Driver LP-11 after HS Burst	$T_{HS-EXIT}$	100	-	-	ns

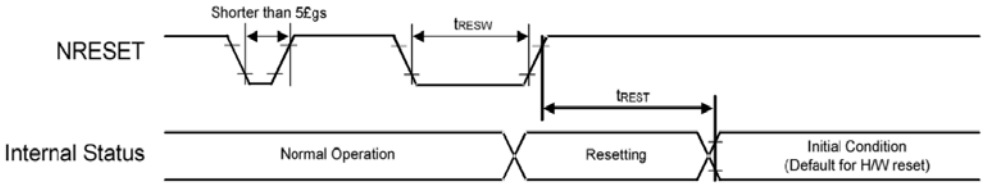
DSI Low Power Mode to High Speed Mode Timing



Signal	Item	Symbol	Spec.			Unit
			Min.	Typ.	Max.	
DSI_CP/ DSI_CN	Time that the MCU shall continue sending HS clock after the last associated Data Lane has transitioned to LP mode	$T_{CLK-POST}$	60+52xUI	-	-	ns
	Time to drive HS differential state after last payload clock bit of a HS transmission burst	$T_{CLK-TRAIL}$	60	-	-	ns
	Time to drive LP-11 after HS burst	$T_{HS-EXIT}$	100	-	-	ns
	Time to drive LP-00 to prepare for HS transmission	$T_{CLK-PREPARE}$	38	-	95	ns
	Time-out at Clock Lane Display Module to enable HS Termination	$T_{CLK-TERM-EN}$	-	-	38	ns
	Minimum lead HS-0 drive period before starting Clock	$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	300	-	-	ns
	Time that the HS clock shall be driven prior to any associated data Lane beginning the transition from LP to HS mode	$T_{CLK-PRE}$	8xUI			

Clock Lanes High Speed Mode to/from Low Power Mode Timing

6. Reset timing



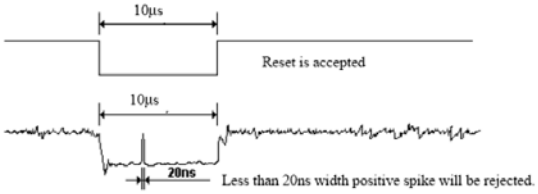
Symbol	Parameter	Related Pins	Spec.			Note	Unit
			Min.	Typ.	Max.		
tRESW	Reset low pulse width(1)	NRESET	10	-	-	-	µs
tREST	Reset complete time(2)	-	15	-	-	When reset applied during SLPIN mode	ms
		-	120	-	-	When reset applied during SLPOUT mode	ms

Notes:

1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (tREST) within 5 ms after a rising edge of NRESET .
2. Spike due to an electrostatic discharge on NRESET line does not cause irregular system reset according to the table below:

NRESET Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 10us	Reset
Between 5us and 10us	Reset starts

3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode.) and then return to Default condition for Hardware Reset.
4. Spike Rejection also applies during a valid reset pulse as shown below:



5. It is necessary to wait 15msec after releasing NRESET before sending commands. Also Sleep Out command cannot be sent for 120msec.

7. Reliability Test

Environment test conditions are listed as following table.

Items	Required Condition	Note
Temperature Humidity Bias (THB)	Ta=40℃, 80%RH, 240hours	
High Temperature Operation (HTO)	Ts= 70℃, 240hours	
Low Temperature Operation (LTO)	Ta= -20℃, 240hours	
High Temperature Storage (HTS)	Ta= 80℃, 240hours	
Low Temperature Storage (LTS)	Ta= -30℃, 240hours	
Thermal Shock Test (TST)	-20℃/30min, 60℃/30min, 100 cycles	
On/Off Test	On/10sec, Off/10sec, 30,000 cycles	
ESD (ElectroStatic Discharge)	Air Discharge: ± 6KV, 150pF(330Ω) 10 times	

Note 1: The TFT-LCD module will not sustain damage after being subjected to 100 cycles of rapid temperature change. A cycle of rapid temperature change consists of varying the temperature from -10℃ to 50℃, and back again. Power is not applied during the test. After temperature cycling, the unit is placed in normal room ambient for at least 4 hours before power on.

8. Shipping package
(TBD)

9. Mechanical Characteristics