5.5” 1080 x 1920

High brightness color TFT-LCD module

Model: VM05BA V1

Version：01

Date: Sep. 27th, 2022

Note: This specification is subject to change without notice

Customer：_____ **Date：_____**

Approved	**Prepared**
Date:	**Date:**

Contents

RECORD OF REVISION

Version and Date	Page	Old description	New description	Remark
0.1 2022/09/27	All	First Edition for customer		

1. Handling Precautions

1) Since front polarizer is easily damaged, pay attention not to scratch it.
2) Be sure to turn off power supply when inserting or disconnecting from input connector.
3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
7) Do not open or modify the Module Assembly.
8) Do not press the reflector sheet at the back of the module to any directions.
9) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
10) After installation of the TFT Module into an enclosure, do not twist nor bend the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.

2. General Description

2.1 Overview

This specification applies to the Color Active Matrix Liquid Crystal Display composed of a TFT-LCD display a LED backlight system. The screen format is intended to support 1080(H) x 1920(V) screen.

2.2 Features

- High brightness display, 1000nits by LED backlight.
- Long operation lifetime BLU design
- Wide view angle
- Wide operation temperature
- RoHS Compliance

2.3 Application

Industrial applications.

2.4 Display specifications

Items	Unit	Specification
Screen Diagonal	inch	5.5”
Active Area	mm	68.04 (H) X 120.96 (V)
Pixels H x V	pixels	1080 x3(RGB) x 1920
Pixels Pitch	um	86.25 (per one triad) x 86.25
Pixel Arrangement		RGB Vertical stripe
Display mode		Normally black
White luminance (center)	Cd/m^2	1000 (Typ)
Contrast ratio		900:1 (Typ.)
Optical Response Time	msec	30 ms (Typ. On/off)
Normal Input Voltage VDD	Volt	3.3
Power Consumption	Watt	TBD (VDD line=TBD W; LED lines= 3.06 W, TBD)
Weight	Grams	TBD
Physical size	mm	75.0(W)× 137.0 (H)× 4.3 (D, typ)
Electrical Interface		MIPI
Support colors		16.7M colors (8 bits)
Temperature range Operating Storage	 ^0C ^0C	 -20 ~ 70 (TFT surface) -20 ~ 70
RoHS Compliance		RoHS Compliance

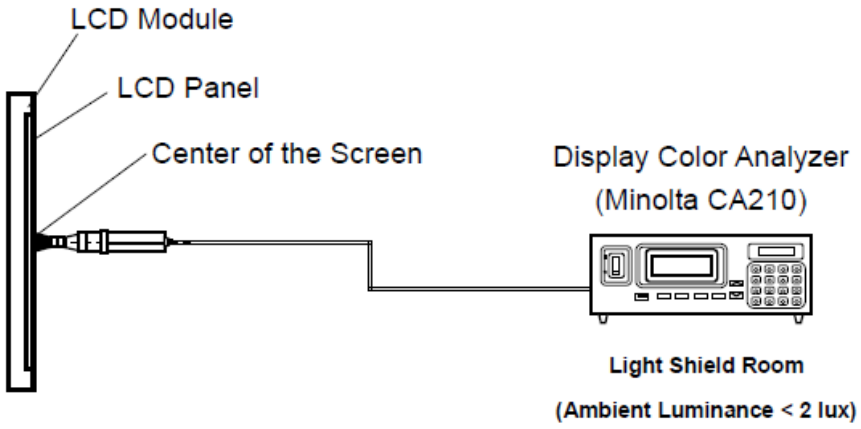
2.5 Optical characteristics

The following optical characteristics are measured under stable condition at 25 ^{0}C

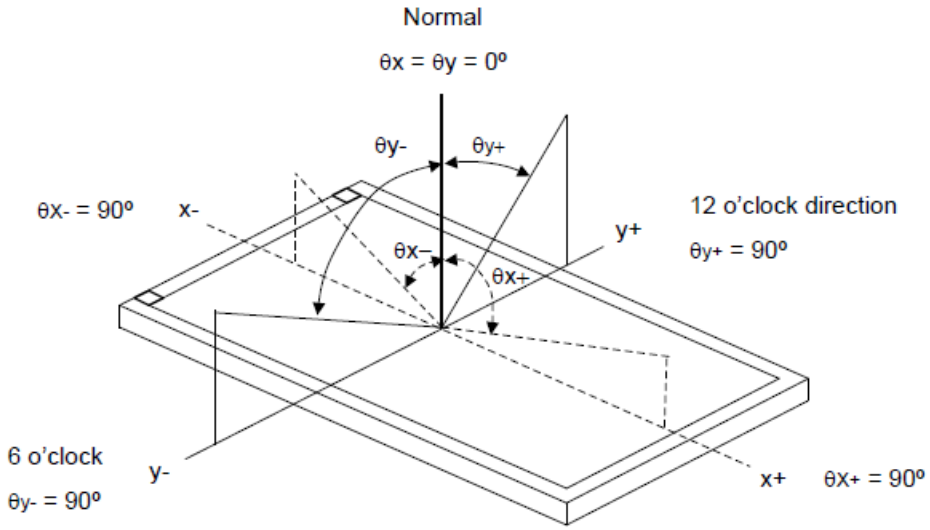
Items	Unit	Conditions	Min.	Typ.	Max.	Note
Viewing angle	Deg.	Horizontal (Right)	70	80		2
		CR=10 (Left)	70	80		
		Vertical (Up)	70	80		
		CR=10 (Down)	70	80		
Contrast Ratio		Normal Direction	600	900		3
Response Time	msec	Raising + Falling		30	35	4
Color coordinates (CIE) White		White x	-0.05	0.30	+0.05	5
		White y		0.32		
Center Luminance	Cd/m^2		800	1000		6
Luminance Uniformity	%		70	75		7
Crosstalk (in 60 Hz)	%				1.5	
Flicker	dB				-20	

Note 1: Measurement method

The LCD module should be stabilized at given temperature for 0.5 hour to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 1 hour in a windless room.



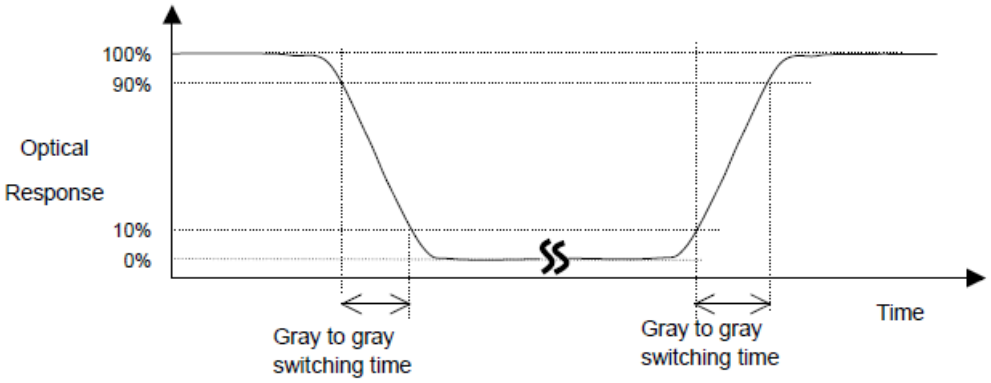
Note 2: Definition of viewing angle



Note 3: Contrast ratio is measured by Minolta CA310

Note 4: Definition of Response time

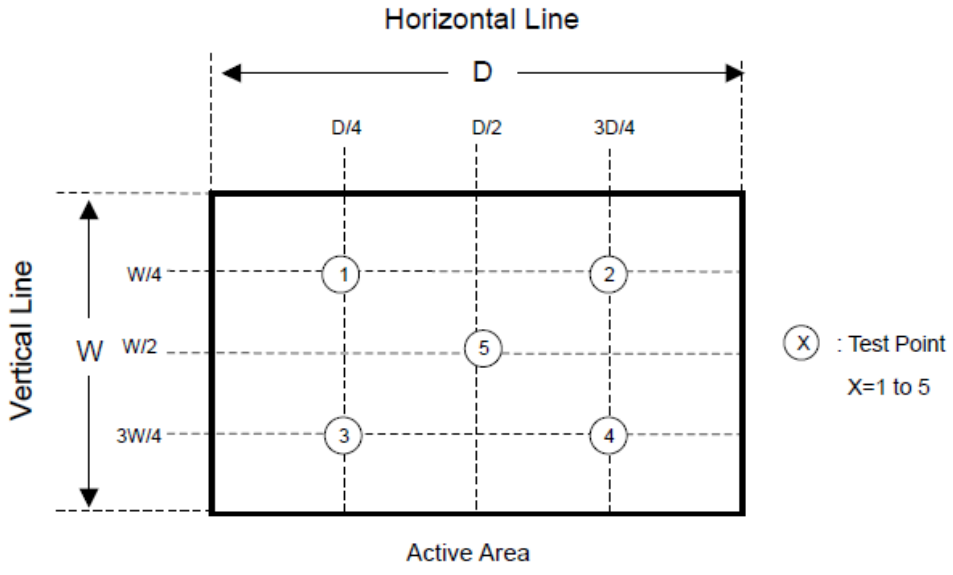
The output signals of photo detector are measured when the input signals are changed from “Full Black” to “Full White” (rising time), and from “Full White” to “Full Black” (falling time), respectively. The response time is interval between the 10% and 90% of amplitudes. Please refer to the figure as below.



Note 5: Color chromaticity and coordinates (CIE) is measured by Minolta CA310

Note 6: Center luminance is measured by Minolta CA310

Note 7: Luminance uniformity of these 5 points is defined as below and measured by Minolta CA310



Uniformity = (Min. Luminance of 5 points) / (Max. Luminance of 5 points)

3. Absolute Maximum Ratings

Absolute maximum ratings of the module are as following:

3.1 TFT LCD module

Item	Symbol	Values		Unit
		Min.	Max.	
I/O and interface power supply	VDDI~GND	-0.3	+3.8	V
Input voltage from step-up circuit	VSP~GND	-0.3	-7.0	V
Input voltage from step-up circuit	VSN~GND	-0.3	+7.0	V

3.2 Environment

Items	Symbol	Values			Unit	Conditions
		Min.	Typ.	Max.		
Operation temperature	T_{OS}	-20	-	70	^{0}C	Note 3
Operation Humidity	H_{OP}	10		85	%	
Storage temperature	T_{ST}	-20		70	^{0}C	
Storage Humidity	H_{ST}	5		90	%	

Note 1: With in Ta= 25℃

Note 2: Permanent damage to the device may occur if exceed maximum values

Note 3: For quality performance, please refer to IIS (Incoming Inspection Standard).

4. Electrical characteristics

4.1 LCD electronics specification

4.1.1 Power specification

Item	Symbol	Values			Unit
		Min.	Typ.	Max.	
Supply Voltagefor IO	VDDI	1.65	1.8	3.6	V
Analog Supply Voltage	VCI	2.5	2.8	3.6	
Input voltage from step-up circuit	VSP	4.5	5.0	6.6	V
Input voltage from step-up circuit	VSN	-6.6	-5.0	-4.5	V
Current Consumption	I_{VDDI}	-	40	60	mA
	I_{VSP}	-	12	20	mA
	I_{VSN}	-	12	20	mA

4.2 Backlight unit

Item	Symbol	Condition	Min	Typ	Max	Unit
Forward Voltage	Vf		16.2	18		V
Uniformity (with L/G)	ΔB_p			75	-	%
Luminance for LCM	/	If=(170mA)	800	1000	-	cd/m^2
Backlight Power Consumption	WBL	If=(170mA)	-	(3.06)	-	W
Backlight lifetime	T	25°C	-	50000	-	hrs
Backlight Color	White					

4.3 Interface connector

4.3.1 TFT connector(CN1)

PIN NO.	Symbol	Description
1	NC	NC
2	GND	Ground
3	GND	Ground
4	GND	Ground
5	GND	Ground
6	GND	Ground
7	NC	NC
8	NC	NC
9	VCI	Analog power supply 2.8V
10	VDDI	Power supply for I/O 1.8V
11	NC	No connect
12	NC	NC
13	NC	NC
14	LCD_RST	Global reset pin
15	TE	Analog supply positive voltage (5.0V)
16	NC	Analog supply negative voltage (-5.0V)
17	LCD_ID	LCM ID
18	GND	Ground
19	D0P	+MIPI differential data input
20	D0N	-MIPI differential data input
21	GND	Ground
22	D1P	+MIPI differential data input
23	D1N	-MIPI differential data input

24	GND	Ground
25	CLKP	MIPI clock positive signal
26	CLKN	MIPI clock negative signal
27	GND	Ground
28	D2P	+MIPI differential data input
29	D2N	-MIPI differential data input
30	GND	Ground
31	D3P	+MIPI differential data input
32	D3N	-MIPI differential data input
33	GND	Ground
34	LEDK1/NC	LED Cathode
35	LEDK2/NC	LED Cathode
36	LEDK3/NC	LED Cathode
37	NC	No connect
38	NC	LED Anode
39	LED+/NC	LED Anode

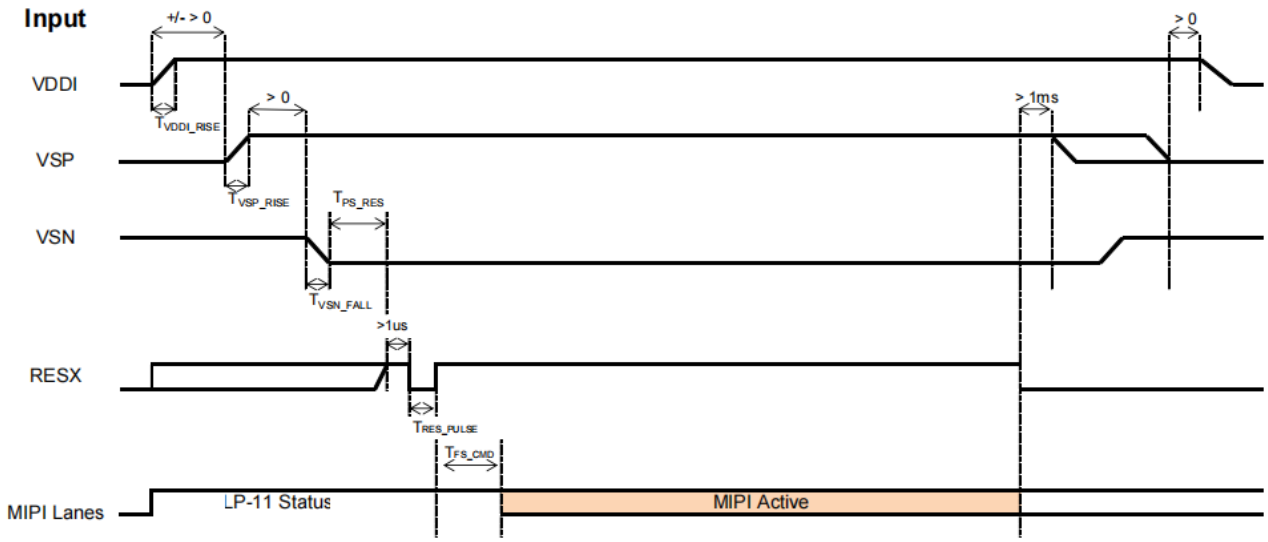
4.3.2 Backlight connector(CN2

Recommended connector : BHSR-02VS-1 manufactured by JST

Pin no	Symbol	I/O	Description	Remark
1	VLED+	P	Backlight LED anode	
2	VLED-	P	Backlight LED cathode	

5. Signal characteristics

5.1 Power sequence



Symbol	Characteristics	Min.	Typ.	Max.	Units
T_{VDDI_RISE}	VDDI Rise time	20	-	-	us
T_{VCI_RISE}	Case A: VCI Rise time	200	-	-	us
	Case B: VCI Rise time	40			
T_{PS_RES}	VDDI/VCI on to Reset high	5	-	-	ms
T_{RES_PULSE}	Reset low pulse time	10	-	-	us
T_{FS_CMD}	Reset to first command	10	-	-	ms

5.2 DC characteristics

5.2.1 For panel driving

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Power & Operation Voltage							
Analog operating voltage	VCI	-	2.5	2.8	6.6	V	
Analog operating voltage	VCIREF		2.5	2.8	6.6	V	
Digital operating voltage	VDDI	-	1.65	2.8	3.6	V	
Digital operating voltage	VCC1		1.65	2.8	6.6	V	
Digital operating voltage	VCC2		1.65	2.8	6.6	V	
DSI operating voltage	VDDAM	-	1.65	1.8	3.6	V	
OTP Supply voltage	MTP_PWR	-	8.4	8.5	8.6	V	
Analog operating voltage	VSP	-	4.5		6.6	V	
Analog operating voltage	VSN	-	-6.6		-4.5	V	
Logic High level input voltage	VIH	-	0.7*VDDI		VDDI	V	Note1
Logic Low level input voltage	VIL	-	-0.3		0.3*VDDI	V	Note1
Logic High level output voltage TE , LEDPWM	VOH	IOH = -1.0mA	0.8*VDDI		VDDI	V	Note1
Logic Low level output voltage TE , LEDPWM	VOL	IOL = +1.0mA	0		0.2*VDDI	V	Note1
Gate Driver High Voltage	VGH	-	8.0	-	18	V	
Gate Driver Low Voltage	VGL	-	-18.0	-	-7.0	V	
Driver Supply Voltage	-	|VGH-VGL|	15	-	32	V	

5.2.2 DSI DC characteristics

The DSI uses different state codes which depend on DC voltage levels of the clock and data lanes. The meaning of the state codes is defined in the following table.

State Code	Line DC Voltage Levels	
	CLOCK_P or DATA_P	CLOCK_N or DATA_N
HS-0	Low (HS)	High (HS)
HS-1	High (HS)	Low (HS)
LP-00	Low (LP)	Low (LP)
LP-01	Low (LP)	High (LP)
LP-10	High (LP)	Low (LP)
LP-11	High (LP)	High (LP)

5.2.2.1 DC characteristics for DSI LP mode

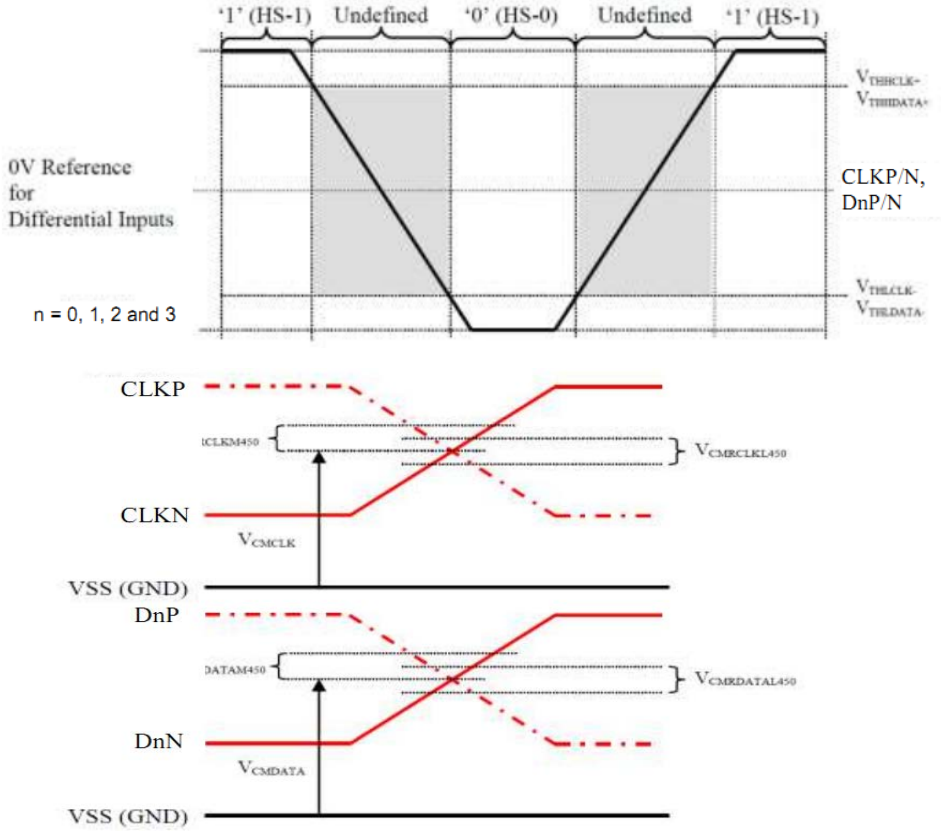
DC levels of the LP-00, LP-01, LP-10 and LP-11 are defined in the table below: DC Characteristics for the DSI LP mode when LP-RX, LP-CD or LP-TX is mentioned in the condition column. Other logical levels in the table are for MCU interface.

Parameter	Symbol	Condition	Specification			Unit
			Min.	Typ.	Max.	
Logic 1 input voltage	V_{IHLPCD}	LP-CD	450	-	1350	mV
Logic 0 input voltage	V_{ILLPCD}	LP-CD	0.0	-	200	mV
Logic 1 input voltage	V_{IHLPRX}	LP-RX (CLK, D0 ,D1, D2, D3)	880	-	1350	mV
Logic 0 input voltage	V_{ILLPRX}	LP-RX (CLK, D0 ,D1, D2, D3)	0.0	-	550	mV
Logic 0 input voltage	$V_{ILLPRXULP}$	LP-RX (CLK ULP mode)	0.0	-	300	mV
Logic 1 output voltage	V_{OHLPTX}	LP-TX (D0)	1.1	-	1.3	V
Logic 0 output voltage	V_{OLLPTX}	LP-TX (D0)	-50	-	50	mV
Logic 1 input current	I_{IH}	LP-CD, LP-RX	-	-	10	uA
Logic 0 input current	I_{IL}	LP-CD, LP-RX	-10	-	-	uA

5.2.2.2 DC characteristics for HS mode

Parameter	Symbol	Condition	Specification			Unit
Input Common Mode Voltage for Clock	V_{CMCLK}	CLKP/N Note 2, Note 3	70	-	330	mV
Input Common Mode Voltage for Data	V_{CMDATA}	DnP/N Note 2, Note 3, Note 5	70	-	330	mV
Common Mode Ripple for Clock Equal or Less than 450MHz	$V_{CMRCLKL450}$	CLKP/N Note 4	-50	-	50	mV
Common Mode Ripple for Data Equal or Less than 450MHz	$V_{CMRDATAL450}$	DnP/N Note 4, Note 5	-50	-	50	mV
Common Mode Ripple for Clock More than 450MHz (peak sine wave)	$V_{CMRCLKM450}$	CLKP/N	-	-	100	mV
Common Mode Ripple for Data More than 450MHz (peak sine wave)	$V_{CMRDATAM450}$	DnP/N Note 5	-	-	100	mV
Differential Input Low Level Threshold Voltage for Clock	$V_{THLCLK-}$	CLKP/N	-70	-	-	mV
Differential Input Low Level Threshold Voltage for Data	$V_{THLDATA-}$	DnP/N Note 5	-70	-	-	mV
Differential Input High Level Threshold Voltage for Clock	$V_{THHCLK+}$	CLKP/N	-	-	70	mV
Differential Input High Level Threshold Voltage for Data	$V_{THHDATA+}$	DnP/N Note 5	-	-	70	mV

The DSI receiver (HS mode) understands that there is logical 1 (= HS-1) when a differential voltage is more than VTHH (CLKP/DnP). The DSI receiver (HS mode) understands that there is logical 0 (= HS-0) when a differential voltage is more than VTHL (CLKN/DnN). There is undefined state if the differential voltage is less than VTHH (CLKP/DnP) and less than VTHL (CLKN/DnN). A reference figure is below.

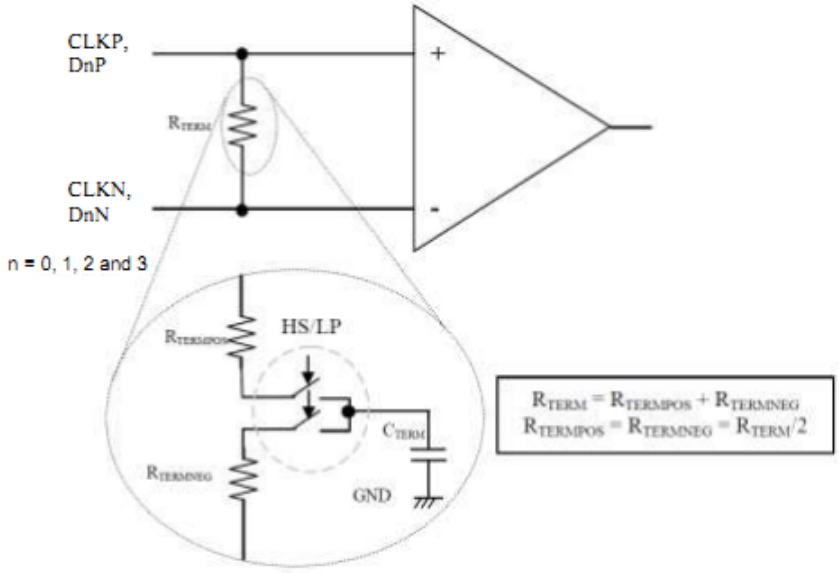


Note: *n = 0, 1, 2 and 3*

The termination resistor (RTERM) of the differential DSI receiver can be driven to two different states by the receiver:

- Low Power (LP) mode when the termination resistor is not connected between differential inputs (CLKP <=> CLKN or D0P <=> D0N or D1P <=> D2N or D2P <=> D3N or D1P <=> D3N)
- High Speed (HS) mode when the termination resistor is connected between differential inputs (CLKP <=> CLKN or D0P <=> D0N or D1P <=> D2N or D2P <=> D3N or D1P <=> D3N)

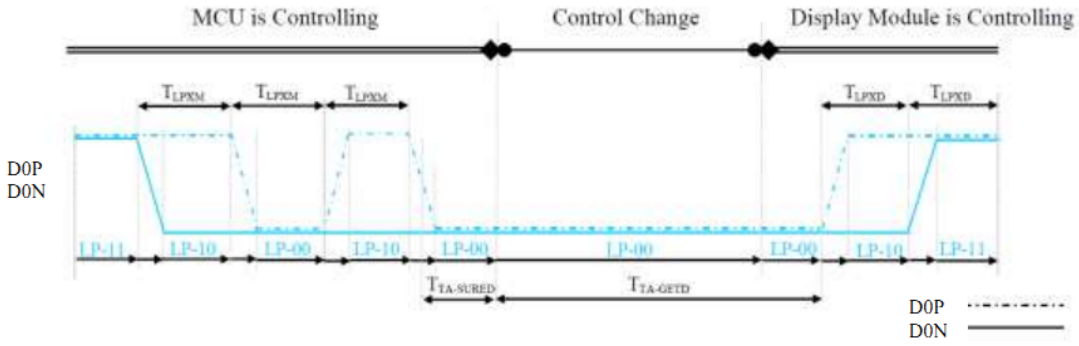
The termination switch (HS/LP), when the termination resistor is not connected, is illustrated below.



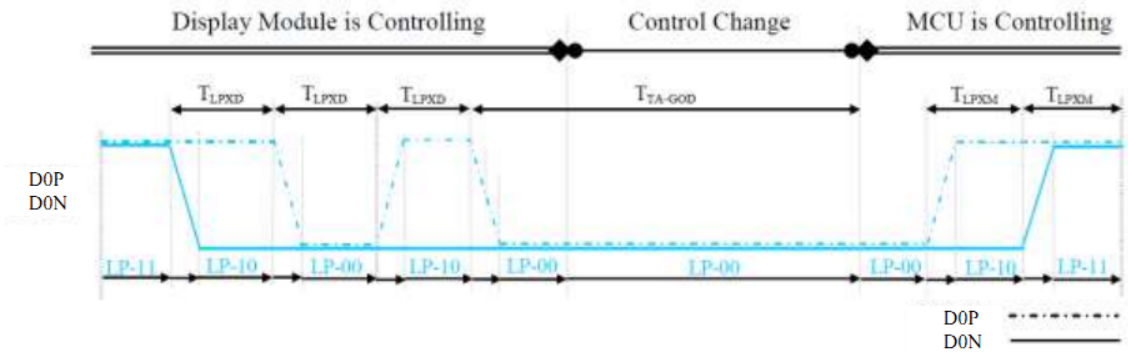
5.3 AC characteristics

5.3.1 Low speed mode

Lower Power Mode and its State Periods on the Bus Turnaround (BTA) from the MCU to the Display Module (ILI9881C) are illustrated for reference purposes below.

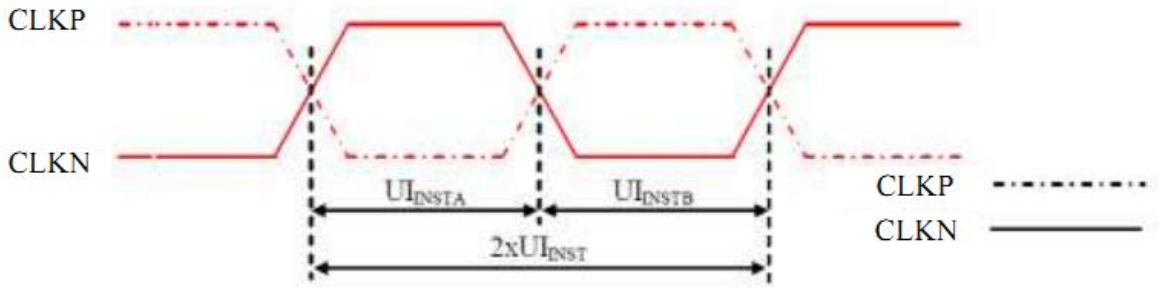


Lower Power Mode and its State Periods on the Bus Turnaround (BTA) from the Display Module (ILI9881C) to the MCU are illustrated for reference purposes below.



5.3.2 High speed mode

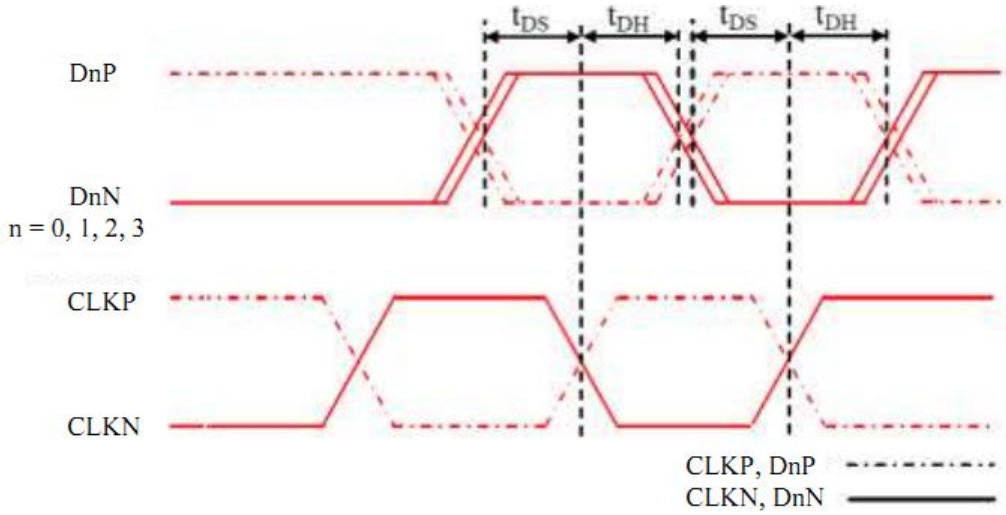
5.3.2.1 Clock channel timing



Signal	Symbol	Parameter	Min	Max	Unit
CLKP/N	$2xUI_{INST}$	Double UI instantaneous	*Note 2*	25	ns
CLKP/N	UI_{INSTA}, UI_{INSTB} (Note 1)	UI instantaneous Half	*Note 2*	12.5	ns

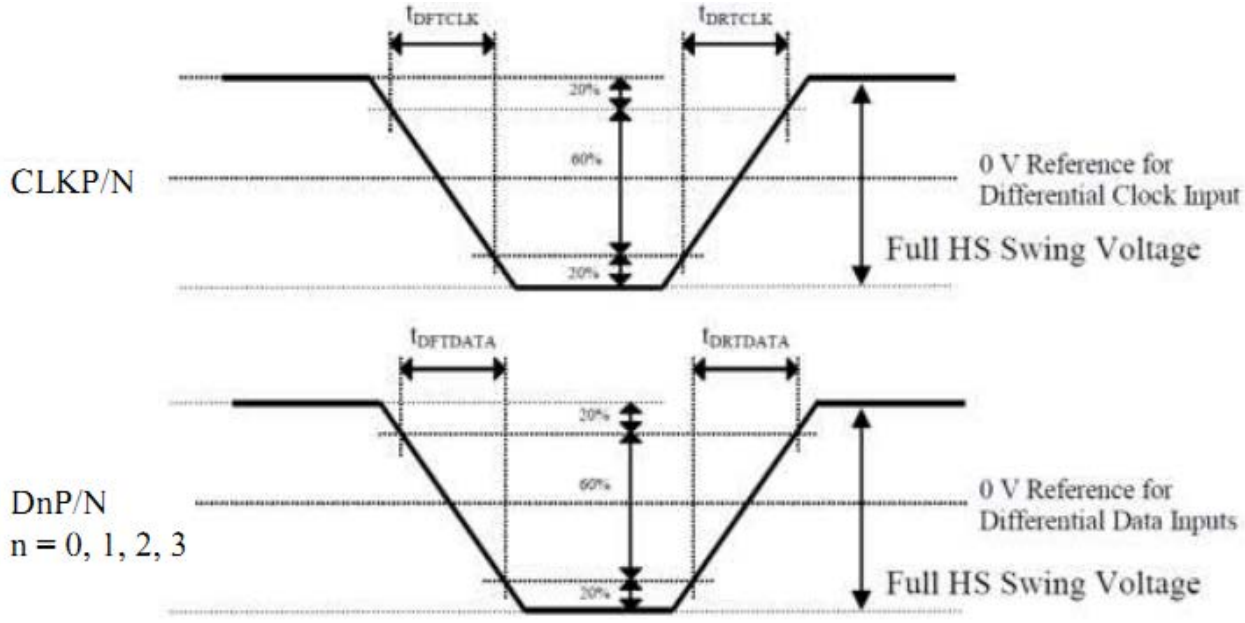
Data type	Two Lanes speed	Three Lanes speed	Four Lanes speed
Data Type = 00 1110 (0Eh), RGB 565, 16 UI per Pixel	566 Mbps	466 Mbps	366 Mbps
Data Type = 01 1110 (1Eh), RGB 666, 18 UI per Pixel	637 Mbps	525 Mbps	412 Mbps
Data Type = 10 1110 (2Eh), RGB 666 Loosely, 24 UI per Pixel	850 Mbps	700 Mbps	550 Mbps
Data Type = 11 1110 (3Eh), RGB 888, 24 UI per Pixel	850 Mbps	700 Mbps	550 Mbps

5.3.2.2 Data clock channel timing



Signal	Symbol	Parameter	Min	Max
DnP/N , n=0 and 1	t_{DS}	Data to Clock Setup time	0.15xUI	-
	t_{DH}	Clock to Data Hold Time	0.15xUI	-

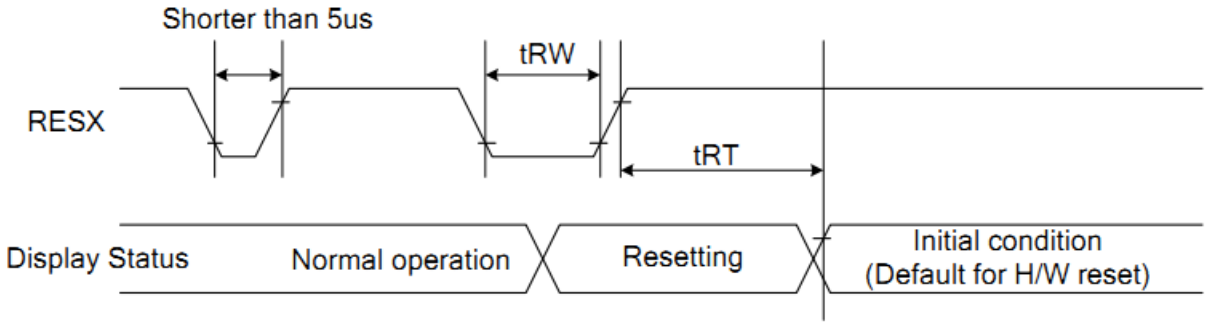
5.3.2.3 High speed mode rising and falling timings



Parameter	Symbol	Condition	Specification		
			Min	Typ	Max
Differential Rise Time for Clock	t_{DRTCLK}	CLKP/N	150 ps	-	0.3UI (Note)
Differential Rise Time for Data	$t_{DRTDATA}$	DnP/N n=0 and 1	150 ps	-	0.3UI (Note)
Differential Fall Time for Clock	t_{DFTCLK}	CLKP/N	150 ps	-	0.3UI (Note)
Differential Fall Time for Data	$t_{DFTDATA}$	DnP/N n=0 and 1	150 ps	-	0.3UI (Note)

Note: *The display module has to meet timing requirements, which are defined for the transmitter (MCU) on MIPI D-Phy standard.*

5.4 Reset timing



Signal	Symbol	Parameter	Min	Max	Unit
RESX	tRW	Reset pulse duration	10		uS
	tRT	Reset cancel		5 (note 1,5)	mS
				120 (note 1,6,7)	mS

6. Reliability Test

Environment test conditions are listed as following table.

Items	Required Condition	Note
Temperature Humidity Bias (THB)	Ta=40℃, 80%RH, 48hours	
High Temperature Operation (HTO)	Ts= 70℃, 48hours	3
Low Temperature Operation (LTO)	Ta= -20℃, 48hours	
High Temperature Storage (HTS)	Ta= 70℃, 48hours	
Low Temperature Storage (LTS)	Ta= -20℃, 48hours	
Thermal Shock Test (TST)	-20℃/30min, 60℃/30min, 100 cycles	
On/Off Test	On/10sec, Off/10sec, 30,000 cycles	
ESD (ElectroStatic Discharge)	Contact Discharge: ± 4KV, 150pF(330Ω) 1sec/cycle	
	Air Discharge: ± 8KV, 150pF(330Ω) 1sec/cycle	

Note 1: The TFT-LCD module will not sustain damage after being subjected to 100 cycles of rapid temperature change. A cycle of rapid temperature change consists of varying the temperature from -10℃ to 50℃, and back again. Power is not applied during the test. After temperature cycling, the unit is placed in normal room ambient for at least 4 hours before power on.

Note 2: According to EN61000-4-2 , ESD class B: Some performance degradation allowed. No data lost. Self-recoverable. No hardware failures.

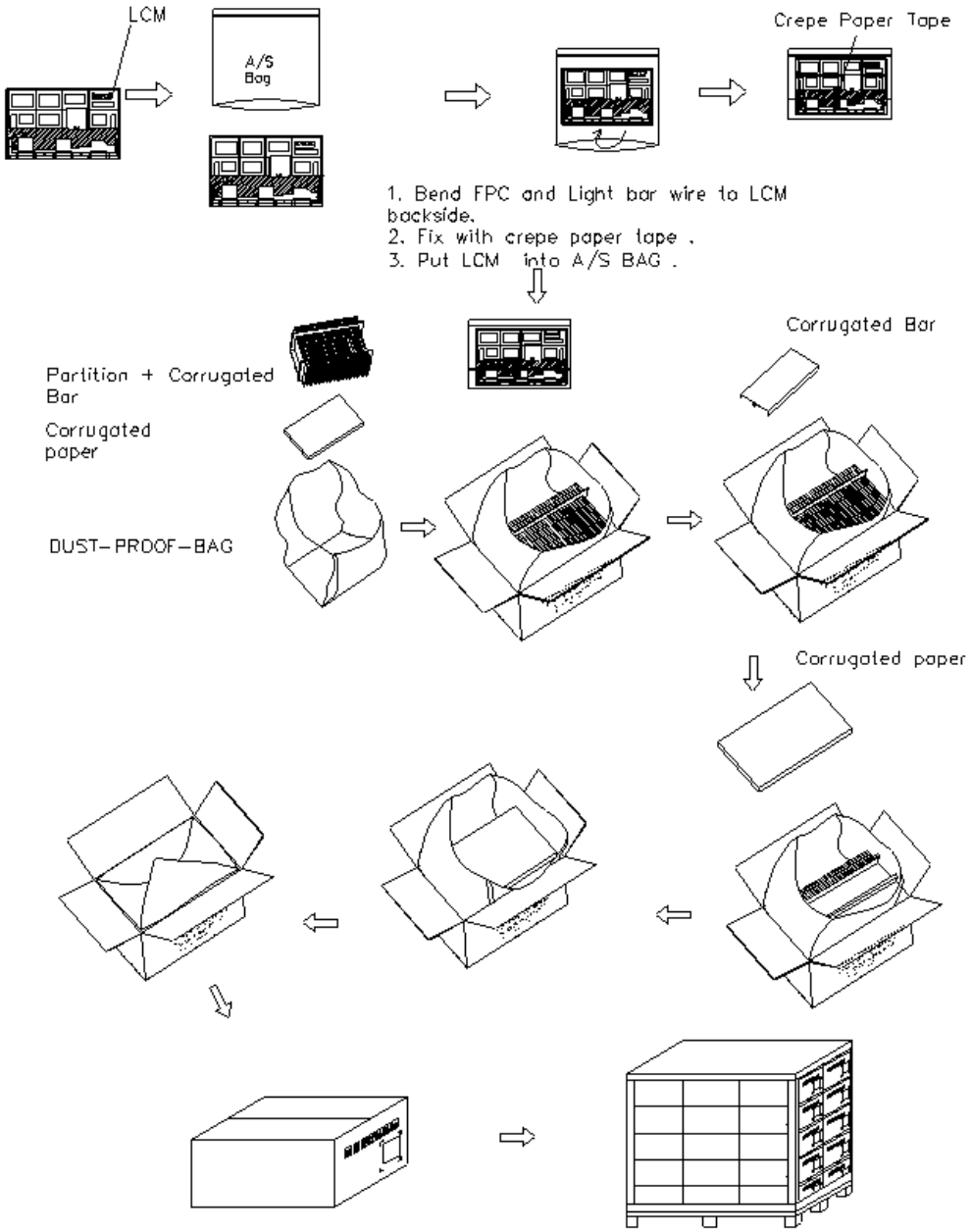
Note 3: TFT surface.

Note 4: There should be no condensation on the surface of panel during test.

Note 5: In the standard conditions, there is no function failure issue occurred. All the cosmetic specification is judged before reliability test.

Note 6: Before cosmetic and function test, the product must have enough recovery time, at least 4 hours at room temperature.

7. Shipping package
(TBD)



8. Mechanical Characteristics