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Product Specification

Applied Green Light, Inc.

7.0" WVGA

High brightness color TFT-LCD module

Model: VM07B4 VB

Date: Jun. 17th, 2022

Note: This specification is subject to change without notice

Customer：_____

Date：_____

Approved	Prepared
Date:	**Date:**

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Contents

RECORD OF REVISION

Version and Date	Page	Old description	New description	Remark
0.1 2022/06/17	All	First Edition for customer		

1. Handling Precautions

1) Since front polarizer is easily damaged, pay attention not to scratch it.

2) Be sure to turn off power supply when inserting or disconnecting from input connector.

3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.

4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.

5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard
   surface.

6) Since CMOS LSI is used in this module, take care of static electricity and insure human
   earth when handling.

7) Do not open or modify the Module Assembly.

8) Do not press the reflector sheet at the back of the module to any directions.

9) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the
   Interface Connector of the TFT Module.

10) After installation of the TFT Module into an enclosure, do not twist nor bend the TFT
    Module even momentary. At designing the enclosure, it should be taken into consideration
    that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the
    TFT Module may be damaged.

2. General Description

2.1 Overview

This specification applies to the Color Active Matrix Liquid Crystal Display composed of a TFT-LCD display a LED backlight system. The screen format is intended to support WVGA (800(H) x 480(V)) and 262K / 16.7 M colors.

LED driving board for backlight unit is not included.

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2.2 Features

- Sunlight readable display, 2000nits by LED backlight.

- Wide viewing angle

- Low power consumption

- Wide operation temperature

- RoHS Compliance

2.3 Application

Industrial Application

2.4 Display specifications

| Items	Unit	Specification
Screen Diagonal	inch	7.0
Active Area	mm	152.4 (H) x 91.44 (V)
Pixels H x V	pixels	800 x3(RGB) x 480
Pixels Pitch	um	190.5(H) x 190.5 (V)
Pixel Arrangement		RGB Vertical stripe
Display mode		Normally black
White luminance (center)	Cd/m^2	2000 (Typ.)
Contrast ratio		800 (Typ.)
Optical Response Time	msec	25 ms (Typ. on/off)
Normal Input Voltage Vcc	Volt	3.3
Power Consumption (Vcc Line + LED backlight)	Watt	6.24 W (Vcc line=0.48 W , LED line=5.76 W)
Weight	Grams	182.8 max.
Physical size	mm	170(H) x 110(V) x 6 / 8.91(D, w/o, w/ PCB)
Electrical Interface		1 Chanel LVDS
Support Colors		262K / 16.7 M colors
Surface Treatment		Anti-Glare, 3H
Temperature range		
Operating	^{0}C	-30 ~ 85 (TFT surface)
Storage (Shipping)	^{0}C	-40 ~ 90
RoHS Compliance		RoHS Compliance

2.5 Optical characteristics

The following optical characteristics are measured under stable condition at 25 ^{0}C

Items	Unit	Conditions	Min.	Typ.	Max.	Note
Viewing angle	Deg.	Horizontal (Right)	80	89		2
		CR=10 (Left)	80	89		
		Vertical (Up)	80	89		
		CR=10 (Down)	80	89		
Contrast Ratio		Normal Direction	600	800		3
Response Time	msec	Raising time (T_{rR})		13		4
		Falling time (T_{rF})		12		
		Raising + Falling		25		
Color / Chromaticity Coordinates (CIE)		Red x	-0.05	0.625	+0.05	5
		Red y		0.303		
		Green x		0.307		
		Green y		0.630		
		Blue x		0.150		
		Blue y		0.050		
Color coordinates (CIE) White		White x		0.313		
		White y		0.329		
Center Luminance	Cd/m^2		1600	2000		6
Luminance Uniformity	%		70	75		7
Crosstalk (in 60 Hz)	%				1.5	
Flicker	dB				-20	

Note 1: Measurement method

The LCD module should be stabilized at given temperature for 0.5 hour to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 1 hour in a windless room.

Note 2: Definition of viewing angle

Note 3: Contrast ratio is measured by Minolta CA 210

Note 4: Definition of Response time

The output signals of photo detector are measured when the input signals are changed from "Full Black" to "Full White" (rising time), and from "Full White" to "Full Black" (falling time), respectively. The response time is interval between the 10% and 90% of amplitudes. Please refer to the figure as below.
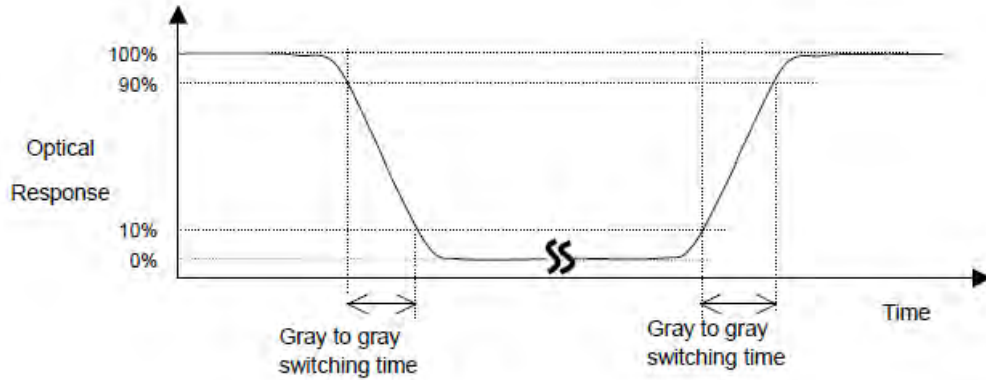
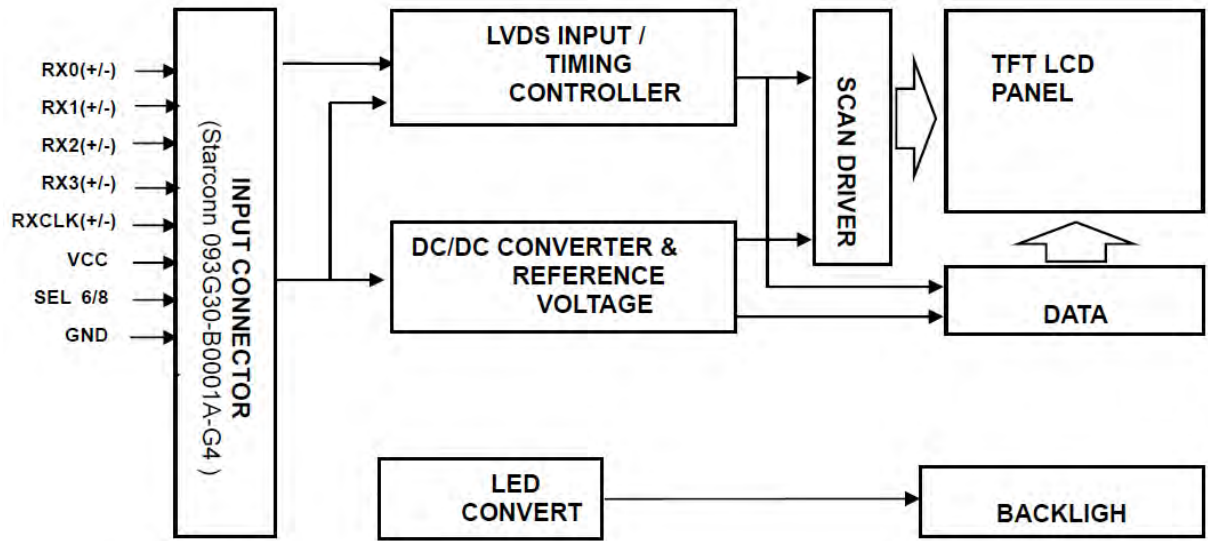Note 5: Color chromaticity and coordinates (CIE) is measured by Minolta CA 210

Note 6: Center luminance is measured by Minolta CA 210

Note 7: Luminance uniformity of these 5 points is defined as below and measured by Minolta CA 210
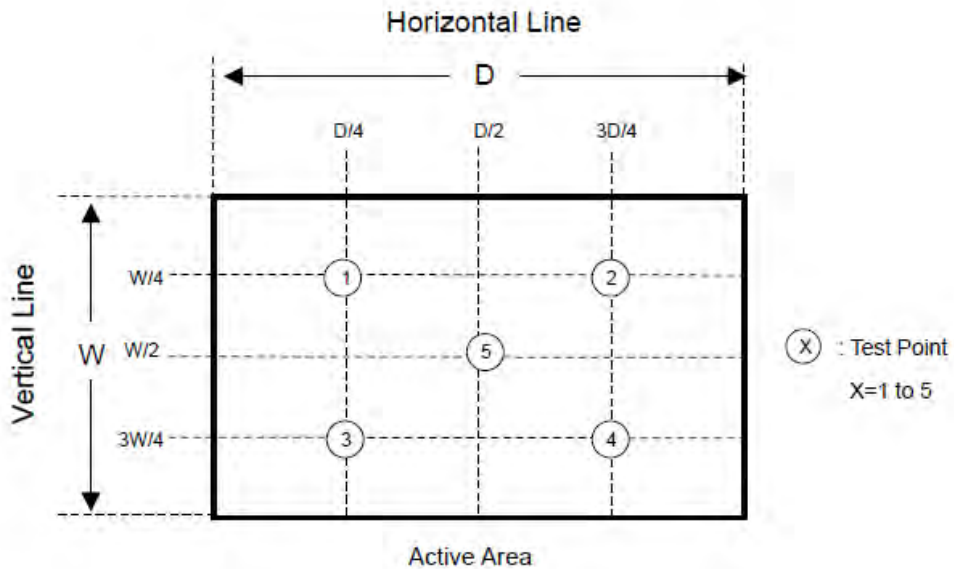
Uniformity = (Min. Luminance of 5 points) / (Max. Luminance of 5 points)

3. Functional Block Diagram

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4. Absolute Maximum Ratings

Absolute maximum ratings of the module are as following:

4.1 TFT LCD module

Items	Symbol	Min	Max	Unit	Conditions
Logic input voltage	V_{CC}	-0.3	3.6	Volt	
Power supply voltage	V_{IN}	-0.3	3.6	Volt	

4.2 Backlight Unit

Items	Symbol	Min	Max	Unit	Conditions
LED Current	I_{LED}	--	600	mA	Note 1, 2

4.3 Environment

Items	Symbol	Values			Unit	Conditions
		Min.	Typ.	Max.		
Operation temperature	T_{OP}	-30	-	85	^0C	
Operation Humidity	H_{OP}	20		80	%	
Storage temperature	T_{ST}	-40		90	^0C	Note 3
Storage Humidity	H_{ST}	30		80	%	

Note 1: With in Ta= 25℃

Note 2: Permanent damage to the device may occur if exceed maximum values

Note 3: For quality performance, please refer to IIS (Incoming Inspection Standard).

5. Electrical Characteristics

5.1 TFT LCD module

5.1.1 Power Specification

Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		Vcc	3.0	3.3	3.6	V	-
Ripple Voltage		V_{RP}	-	-	100	mVp-p	-
Rush Current		I_{RUSH}	-	-	2	A	(2)
Power Supply Current	White	-	-	135	200	mA	(3)a
	Black	-	-	85	135	mA	(3)b
	Vertical Stripe	-	-	145	220	mA	(3)c
Power Consumption		PLCD	-	0.48	0.73	W	
LVDS differential input voltage		Vid	200	-	600	mV	
LVDS common input voltage		Vic	1.0	1.2	1.4	V	
LVDS terminating resistor		R_T	-	100	-	ohm	

Note (1) The ambient temperature is Ta = 25 ± 2 ℃.

Note (2) Measurement Conditions:
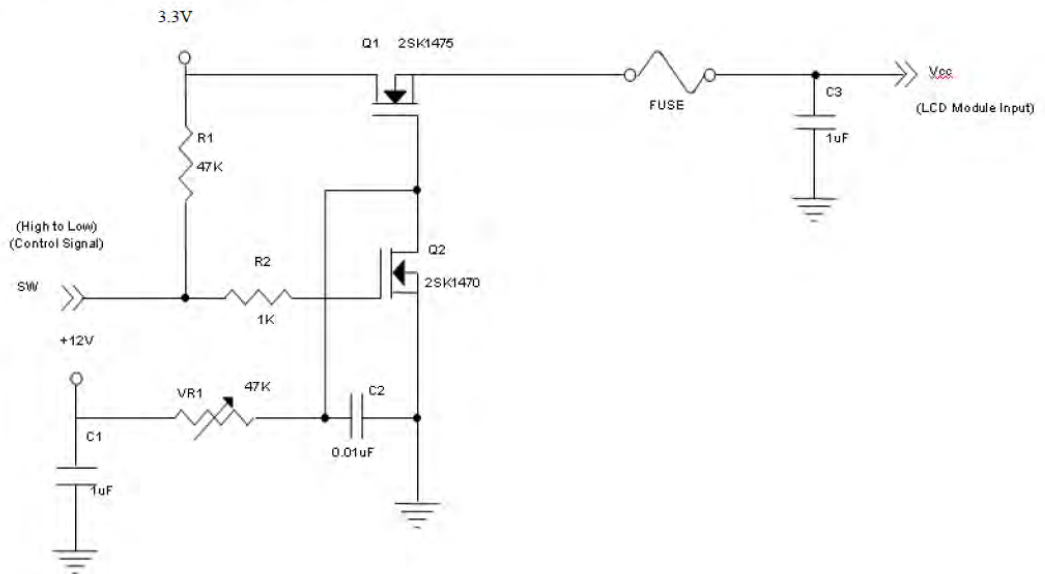
Vcc rising time is 470μs
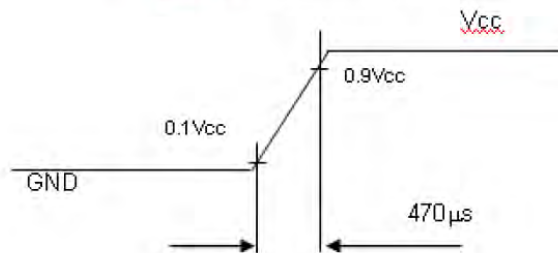
Note (3) The specified power supply current is under the conditions at Vcc = 3.3 V, Ta = 25 ± 2 ℃, Fr = 60Hz, whereas a power dissipation check pattern below is displayed.

a. White Pattern

Active Area

b. Black Pattern

Active Area

c. Vertical Stripe Pattern

Active Area
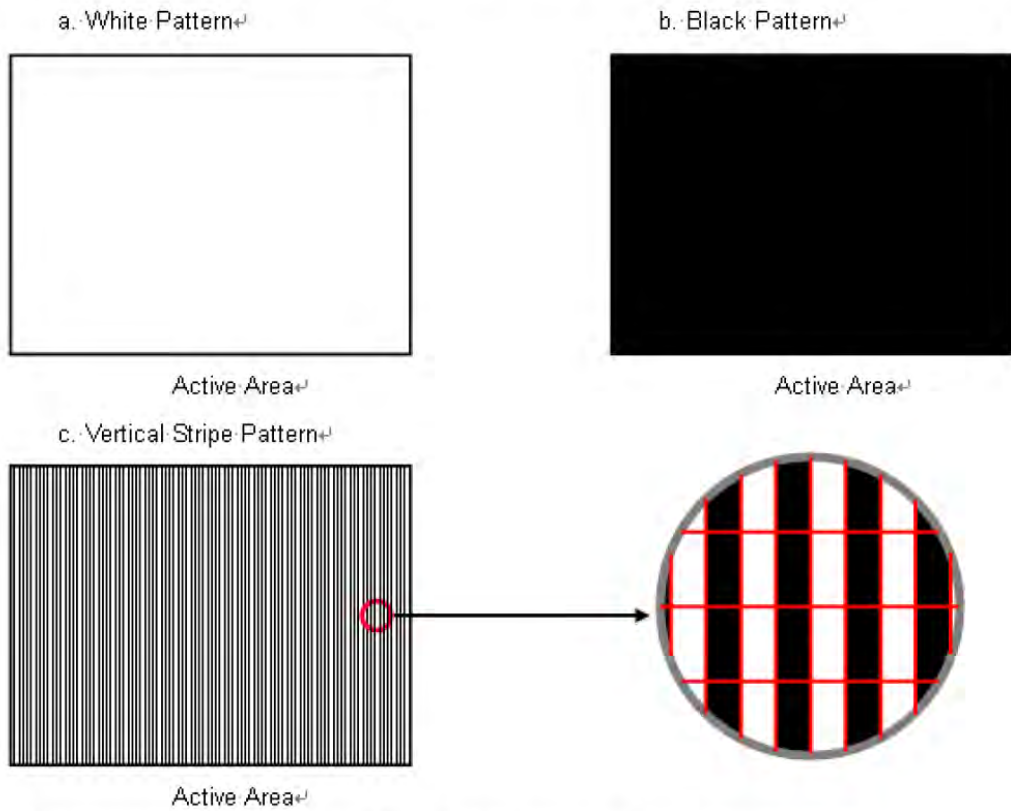
Note (4) The power consumption is specified at the pattern with the maximum current.

Note (5) VID waveform condition

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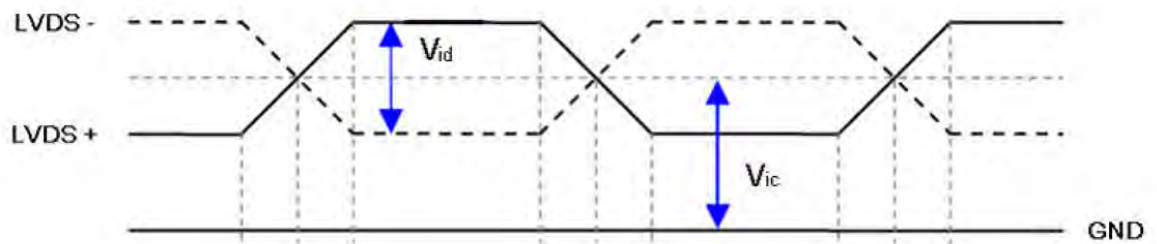
5.2 Backlight unit

Parameter	Min	Typ	Max	Unit	Note
LED voltage (VL)		18		[V]	2
LED current (IL)		320		[mA]	2
LED power (PL)		5.76		[W]	
LED lite time (MTBF)		100,000		[Hour]	1

Note 1: The "LED lift time" is defined as the module brightness decrease to 50% original brightness that the ambient temperature

is 25℃ and typical LED Current at 320 mA

Note 2: The variance of LED Light Bar power consumption is ±10%. Calculator value for reference (IL × VL = PLED)

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5.3 Interface connection

5.3.1 TFT connector (CN1)

PIN ASSIGNMENT

Pin No.	Symbol	Description	Note
1	NC	No Conncetion	-
2	NC	No Conncetion	-
3	NC	No Conncetion	-
4	NC	No Conncetion	-
5	NC	No Conncetion	-
6	NC	No Conncetion	-
7	NC	No Conncetion	-
8	NC	No Conncetion	-
9	VCC	Power supply: +3.3V	-
10	VCC	Power supply: +3.3V	-
11	GND	Ground	-
12	GND	Ground	-
13	RX0-	Negative transmission data of pixel 0	-
14	RX0+	Positive transmission data of pixel 0	-
15	GND	Ground	-
16	RX1-	Negative transmission data of pixel 1	-
17	RX1+	Positive transmission data of pixel 1	-
18	GND	Ground	-
19	RX2-	Negative transmission data of pixel 2	-
20	RX2+	Positive transmission data of pixel 2	-
21	GND	Ground	-
22	RXCLK-	Negative of clock	-
23	RXCLK+	Positive of clock	-
24	GND	Ground	-
25	RX3-	Negative transmission data of pixel 3	-
26	RX3+	Positive transmission data of pixel 3	-
27	GND	Ground	-
28	SEL6/8	LVDS 6/8 bit select function control, Low → 6 bit Input Mode High or NC → 8bit Input Mode	(2)
29	GND	Ground	-
30	GND	Ground	-

Note (1) Connector Part No.: Starconn 093G30-B0001A-G4.

Note (2) "Low" stands for 0V. "High" stands for 3.3V

Note (3) Pin7, Pin8 input signals should be set to no connection or ground, this module would operate normally.

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5.3.2 Backlight connector (CN2)

Recommended connector : JOIN TEK JT1025-1021 (BHSR-02VS-1 manufactured by JST)

| Pin no	Symbol	I/O	Description	Remark
1	VLED+	P	Backlight LED anode	
2	VLED-	P	Backlight LED cathode	

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5.4 LVDS input signal specifications

5.4.1 LVDS data mapping table

The brightness of each primary color (red, green and blue) is based on the 8-bit gray scale data input for the color. The higher the binary input, the brighter the color. The table below provides the assignment of color versus data input.

Color		Data Signal																								
		Red								Green								Blue							
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale Of Red	Red(0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(1)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(2)	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Red(253)	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(254)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Green	Green(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	Green(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green(253)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0
	Green(254)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	Green(255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Gray Scale Of Blue	Blue(0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue(253)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1
	Blue(254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	Blue(255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Note (1) 0: Low Level Voltage, 1: High Level Voltage
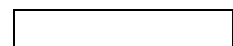
5.5 Display timing specifications

The input signal timing specifications are shown as the following table and timing diagram.

| Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
LVDS Clock	Frequency	Fc	25.2	25.4	35.7	MHz	-
	Period	Tc		39.37		ns	
	Input cycle to cycle jitter	T_{rcl}	-0.02*Tc	-	0.02*Tc	ns	(3)
	Input clock to data skew	TLVCCS	-0.02*Tc	-	0.02*Tc	ns	(4)
	Spread spectrum modulation range	Fclkin_mod	FC*98%	-	FC*102%	MHz	(5)
	Spread spectrum modulation frequency	F_{SSM}	23	-	93	KHz	
Vertical Display Term	Frame Rate	Fr	-	60	-	Hz	Tv=Tvd+Tvb
	Total	Tv	488	490	611	Th	-
	Active Display	Tvd	480	480	480	Th	-
	Blank	Tvb	8	10	131	Th	-
Horizontal Display Term	Total	Th	860	864	974	Tc	Th=Thd+Thb
	Active Display	Thd	800	800	800	Tc	-
	Blank	Thb	60	64	174	Tc	-

Note (1) Because this module is operated by DE only mode, Hsync and Vsync input signals are ignored.

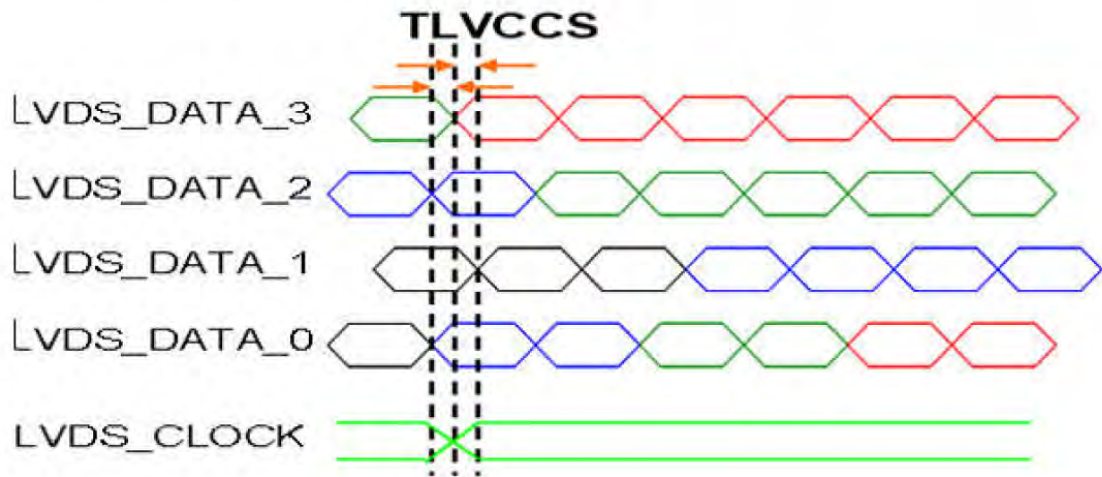Note (2) The Tv(Tvd+Tvb) must be integer, otherwise, this module would operate abnormally.
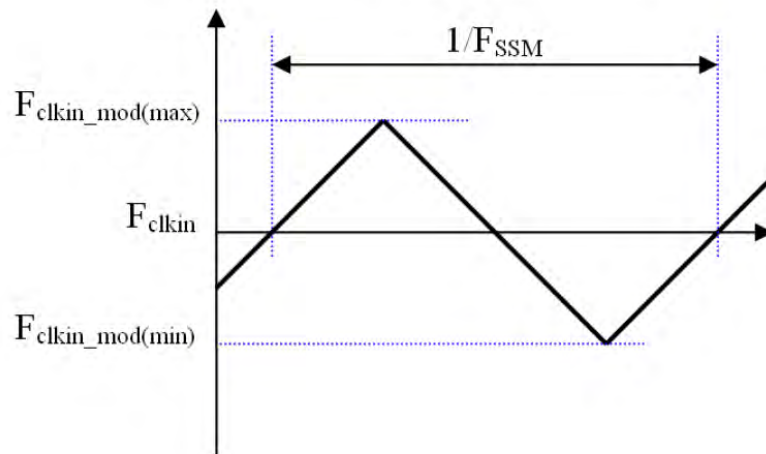
INPUT SIGNAL TIMING DIAGRAM

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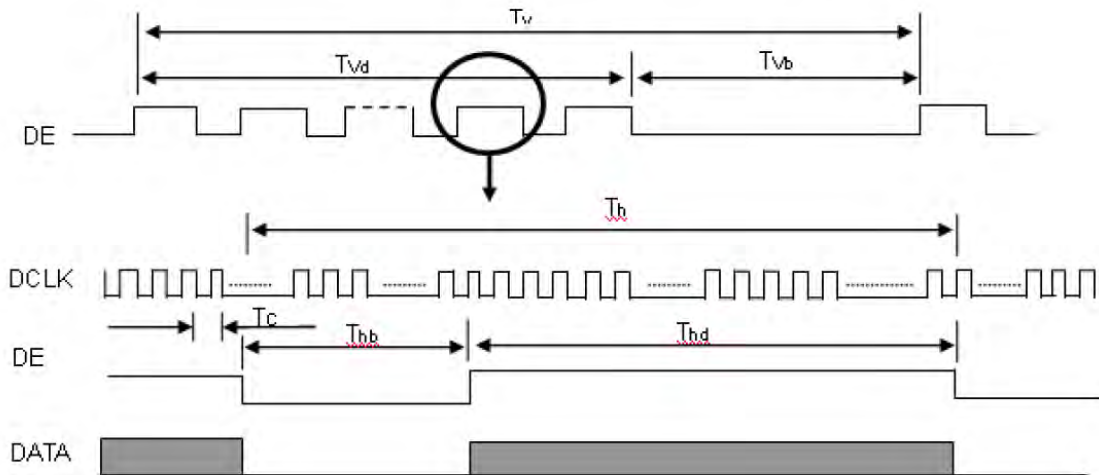
Note (3) The input clock cycle-to-cycle jitter is defined as below figures. Trcl = I T$_1$ – TI
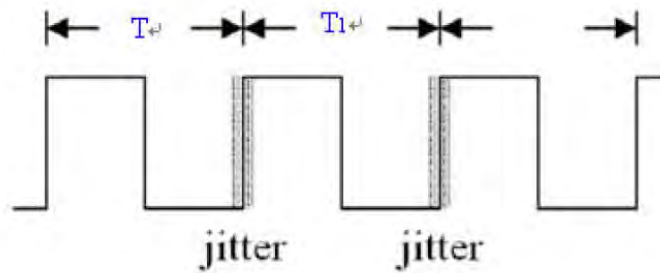
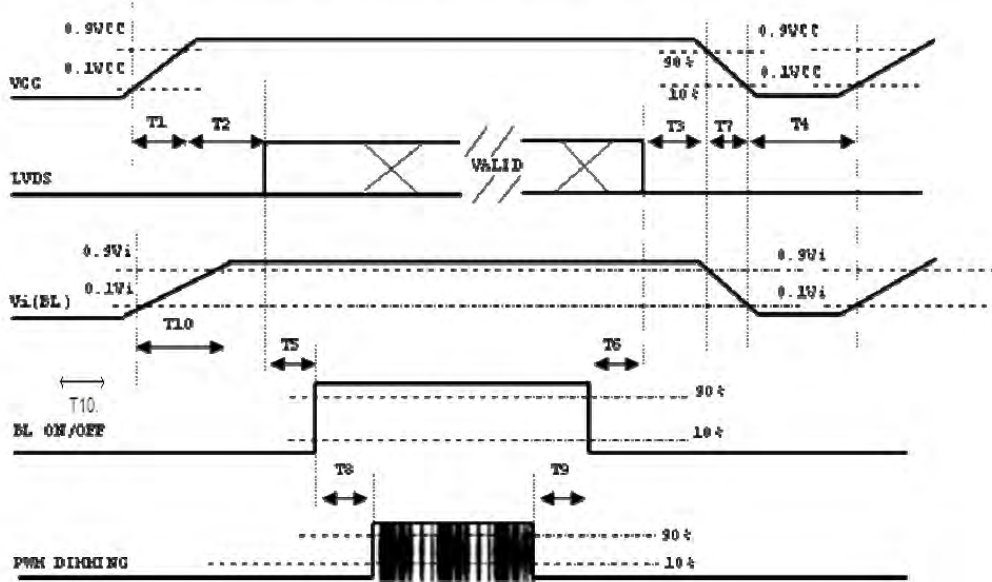Note (4) Input Clock to data skew is defined as below figures.

TLVCCS

Note (5) The SSCG (Spread spectrum clock generator) is defined as below figures.

5.6 Power ON/OFF for LCD

The power sequence specifications are shown as the following table and diagram.

Timing Specifications:

Parameter	Value			Units
	Min	Typ	Max	
T1	0.5	-	10	ms
T2	0	-	50	ms
T3	0	-	50	ms
T4	500	-	-	ms
T5	450	-	-	ms
T6	200	-	-	ms
T7	10	-	100	ms
T8	10	-	-	ms
T9	10	-	-	ms
T10	20		50	

Note (1) Please avoid floating state of interface signal at invalid period.

Note (2) When the interface signal is invalid, be sure to pull down the power supply of LCD VCC to 0 V.

Note (3) The Backlight converter power must be turned on after the power supply for the logic and the interface signal is valid. The Backlight converter power must be turned off before the power supply for the logic and the interface signal is invalid.

6. Reliability Test

Environment test conditions are listed as following table.

Items	Required Condition	Note
Temperature Humidity Bias (THB)	Ta= 50℃, 80%RH, 240hours	
High Temperature Operation (HTO)	Ta= 85℃, 240hours	3
Low Temperature Operation (LTO)	Ta= -30℃, 240hours	
High Temperature Storage (HTS)	Ta= 90℃, 240hours	
Low Temperature Storage (LTS)	Ta= -40℃, 240hours	
Thermal Shock Test (TST)	-10℃/30min, 60℃/30min, 100 cycles	
On/Off Test	On/10sec, Off/10sec, 30,000 cycles	
ESD (ElectroStatic Discharge)	Contact Discharge: ± 8KV, 150pF(330Ω) 1sec, 9 points, 25 times/ point.	
	Air Discharge: ± 15KV, 150pF(330Ω) 1sec 9 points, 25 times/ point.	

Note 1: The TFT-LCD module will not sustain damage after being subjected to 100 cycles of rapid temperature change. A cycle of rapid temperature change consists of varying the temperature from -10℃ to 60℃, and back again. Power is not applied during the test. After temperature cycling, the unit is placed in normal room ambient for at least 4 hours before power on.

Note 2: According to EN61000-4-2 , ESD class B: Some performance degradation allowed. No data lost. Self-recoverable. No hardware failures.

Note 3: TFT surface temperature.

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7. Shipping package (TBD)

(1) 38 pcs LCD modules / 1 Box

(2) Box dimensions: 445 (L) X 370 (W) X 275 (H) mm

(3) Weight: approximately 8.3Kg (38modules per box)

PACKING METHOD

LCD Module

Tape
protect film

Anti-Static Bag

Note:PCBA Downward

(1)Box Dimensions : 445(L)*370(W)*275(H)
(2)38 Modules/Carton

Cushion(bottom)

Note:PCBA Downward

Cushion(up)

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8. Mechanical Characteristics