8.0” 1200 x 1920

High brightness color TFT-LCD module

Model: VM08BA V2

Version：01

Date: Sep. 28th, 2023

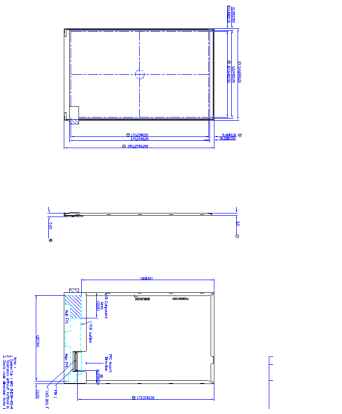
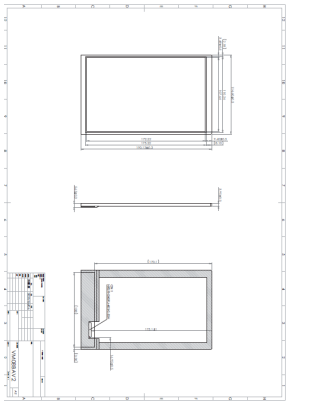
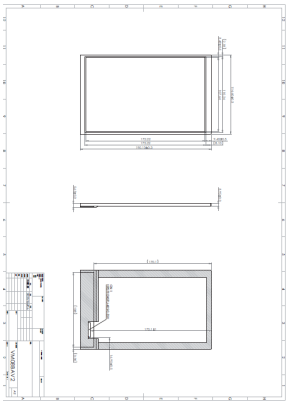
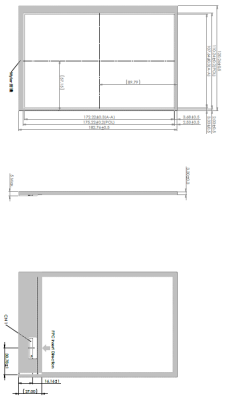
Note: This specification is subject to change without notice

Customer： _____ **Date：** _____

Approved	**Prepared**
Date:	**Date:**

Contents

RECORD OF REVISION

Version and Date	Page	Old description	New description	Remark
0.1 2021/07/30	All	First Edition for customer		
0.2 2023/04/06	26			
0.3 2023/09/28	6	Physical size mm 114.6 (W)× 190.125 (H)× 5.65 (D, w PCB)	Physical size mm 120.26 (W)× 182.76(H)× 5.0 (D, w PCB)	
	19	MTBF 70,000 Hrs	MTBF 100,000 Hrs	
	26			

1. Handling Precautions

1) Since front polarizer is easily damaged, pay attention not to scratch it.
2) Be sure to turn off power supply when inserting or disconnecting from input connector.
3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
7) Do not open or modify the Module Assembly.
8) Do not press the reflector sheet at the back of the module to any directions.
9) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
10) After installation of the TFT Module into an enclosure, do not twist nor bend the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.

2. General Description

2.1 Overview

This specification applies to the Color Active Matrix Liquid Crystal Display composed of a TFT-LCD display a LED backlight system. The screen format is intended to support 1200(H) x 1920(V) screen and 16.7M colors (8 bit).

2.2 Features

- High brightness display, 1500nits by LED backlight.
- Long operation lifetime BLU design
- Wide view angle
- Wide operation temperature
- RoHS Compliance

2.3 Application

Industrial applications.

2.4 Display specifications

Items	Unit	Specification
Screen Diagonal	inch	8.0”
Active Area	mm	107.64 (H) X 172.224 (V)
Pixels H x V	pixels	1200 x3(RGB) x 1920
Pixels Pitch	um	89.7 (per one triad) x 89.7
Pixel Arrangement		RGB Vertical stripe
Display mode		Normally black
White luminance (center)	Cd/m^2	1500 (Typ)
Contrast ratio		900:1 (Typ.)
Optical Response Time	msec	25 ms (Typ. On/off)
Normal Input Voltage VDD	Volt	3.3
Power Consumption (Vcc Line + LED backlight)	Watt	4.815 W (VDD line=0.495 W; LED lines= 4.32 W)
Weight	Grams	TBD
Physical size	mm	120.26 (W)× 182.76(H)× 5.0 (D, w PCB)
Electrical Interface		4 lane MIPI
Support colors		16.7M colors
Surface Treatment		Anti-glare, Hardness 3H
Temperature range Operating Storage	 ^0C ^0C	 -10 ~ 60 (TFT surface) -20 ~ 70
RoHS Compliance		RoHS Compliance

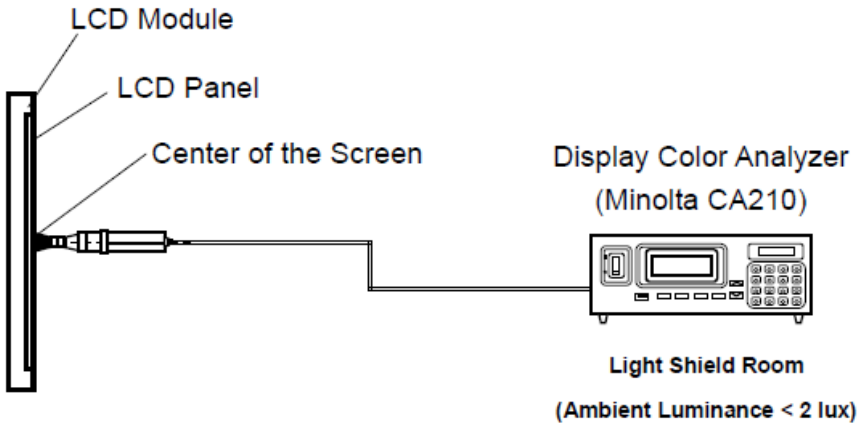
2.5 Optical characteristics

The following optical characteristics are measured under stable condition at 25 ^{0}C

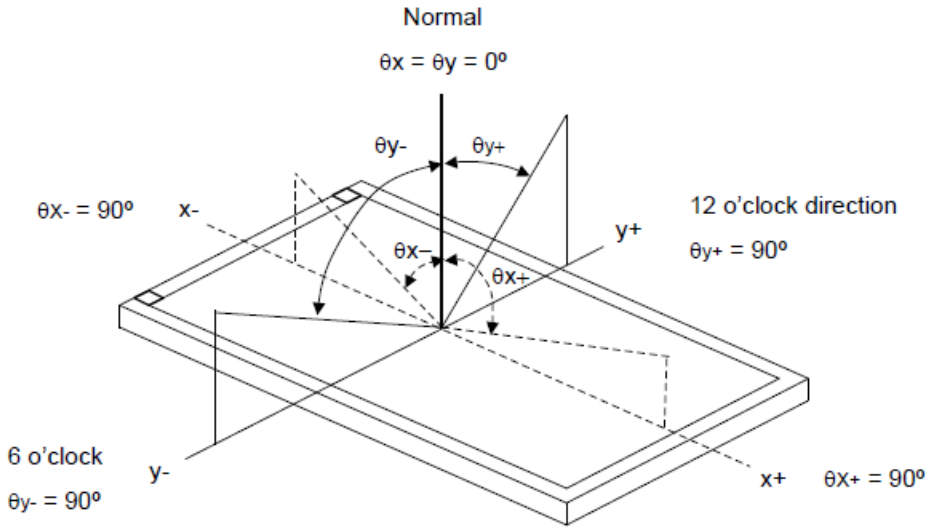
Items	Unit	Conditions	Min.	Typ.	Max.	Note
Viewing angle	Deg.	Horizontal (Right) CR=10 (Left)		85 85		2
		Vertical (Up) CR=10 (Down)		85 85		
Contrast Ratio		Normal Direction		900		3
Response Time	msec	Raising + Falling		25	55	4
Color / Chromaticity Coordinates (CIE)		Red x	-0.05	0.6354	+0.05	5
		Red y		0.3224		
		Green x		0.2731		
		Green y		0.6676		
		Blue x		0.1501		
		Blue y		0.1221		
Color coordinates (CIE) White		White x		0.300		
		White y		0.330		
Center Luminance	Cd/m^2		1200	1500		6
Luminance Uniformity	%		70	75		7
Crosstalk (in 60 Hz)	%				1.5	
Flicker	dB				-20	

Note 1: Measurement method

The LCD module should be stabilized at given temperature for 0.5 hour to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 1 hour in a windless room.



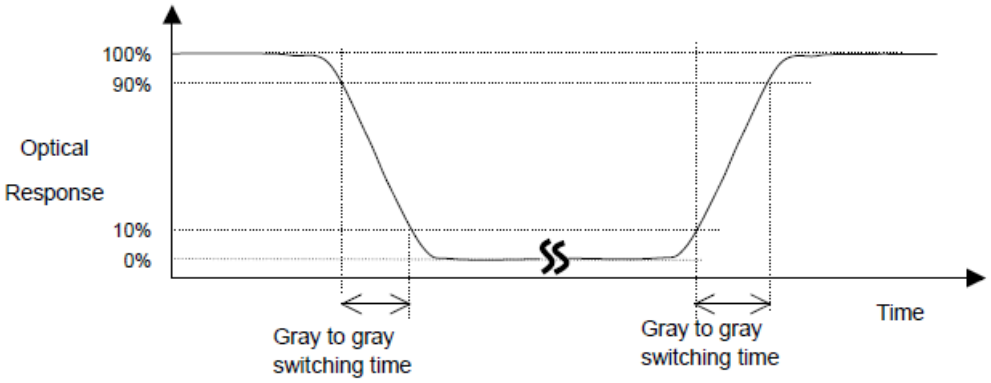
Note 2: Definition of viewing angle



Note 3: Contrast ratio is measured by Minolta CA210

Note 4: Definition of Response time

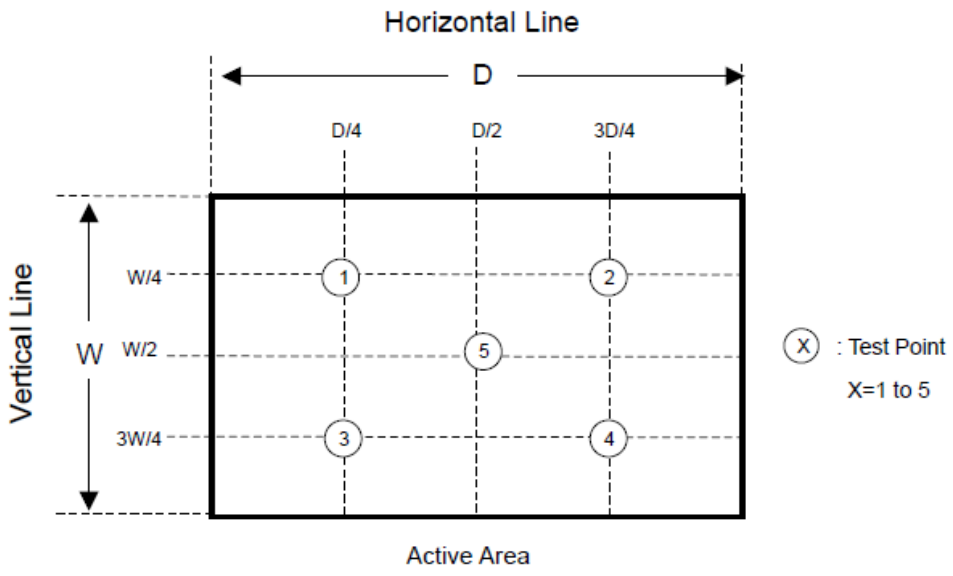
The output signals of photo detector are measured when the input signals are changed from “Full Black” to “Full White” (rising time), and from “Full White” to “Full Black” (falling time), respectively. The response time is interval between the 10% and 90% of amplitudes. Please refer to the figure as below.



Note 5: Color chromaticity and coordinates (CIE) is measured by Minolta CA210

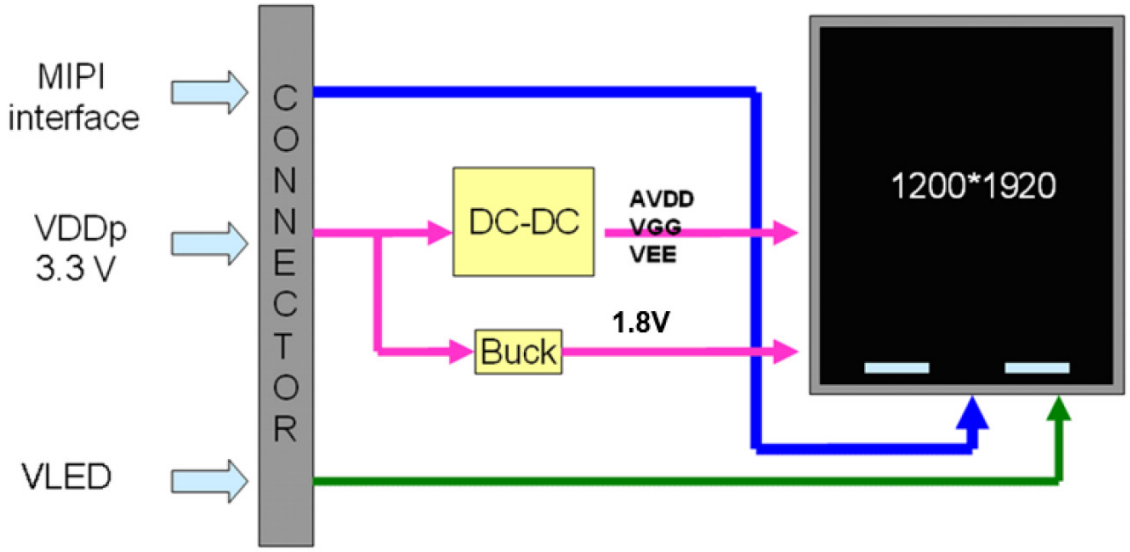
Note 6: Center luminance is measured by Minolta CA210

Note 7: Luminance uniformity of these 5 points is defined as below and measured by Minolta CA210



Uniformity = (Min. Luminance of 5 points) / (Max. Luminance of 5 points)

3. Function block diagram



4. Absolute Maximum Ratings

Absolute maximum ratings of the module are as following:

4.1 TFT LCD module

Items	Symbol	Min	Max	Unit	Conditions
Power supply voltage	V_{DD}	-0.3	4.0	Volt	Note 1, 2

4.2 Backlight unit

Items	Symbol	Min	Max	Unit	Conditions
LED bar input current			600	mA	

4.3 Environment

Items	Symbol	Values			Unit	Conditions
		Min.	Typ.	Max.		
Operation temperature	T_{OS}	-10	-	60	^{0}C	Note 3
Operation Humidity	H_{OP}	10		85	%	
Storage temperature	T_{ST}	-20		70	^{0}C	
Storage Humidity	H_{ST}	5		90	%	

Note 1: With in Ta= 25℃

Note 2: Permanent damage to the device may occur if exceed maximum values

Note 3: For quality performance, please refer to IIS (Incoming Inspection Standard).

5. Electrical characteristics

5.1 LCD electronics specification

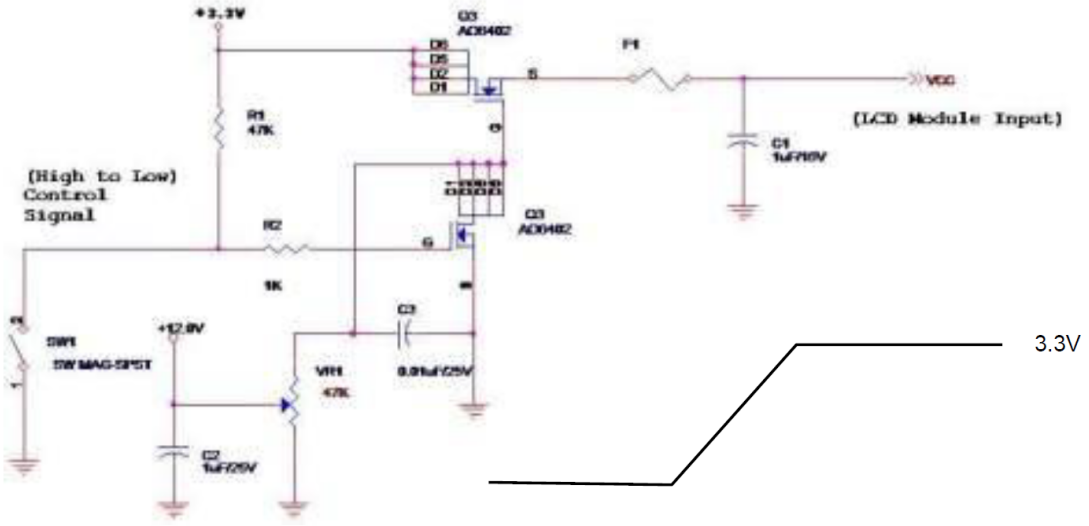
5.1.1 Power specification

The power specification are measured under 25℃ and frame frenquency under 60Hz

Symble	Parameter	Min	Typ	Max	Units	Note
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[Volt]	
PDD	VDD Power	-	-	0.495	[Watt]	Note 1
IDD	IDD Current	-	-	150	[mA]	Note 1
IRush	Inrush Current	-	-	1500	[mA]	Note 2
VDDrp	Allowable Logic/LCD Drive Ripple Voltage	-	-	100	[mV] p-p	

Note 1: Maximum Measurement Condition：White Pattern at 3.3V driving voltage. ($P_{max}=V_{3.3} \times I_{black}$)

Note 2: Measure Condition

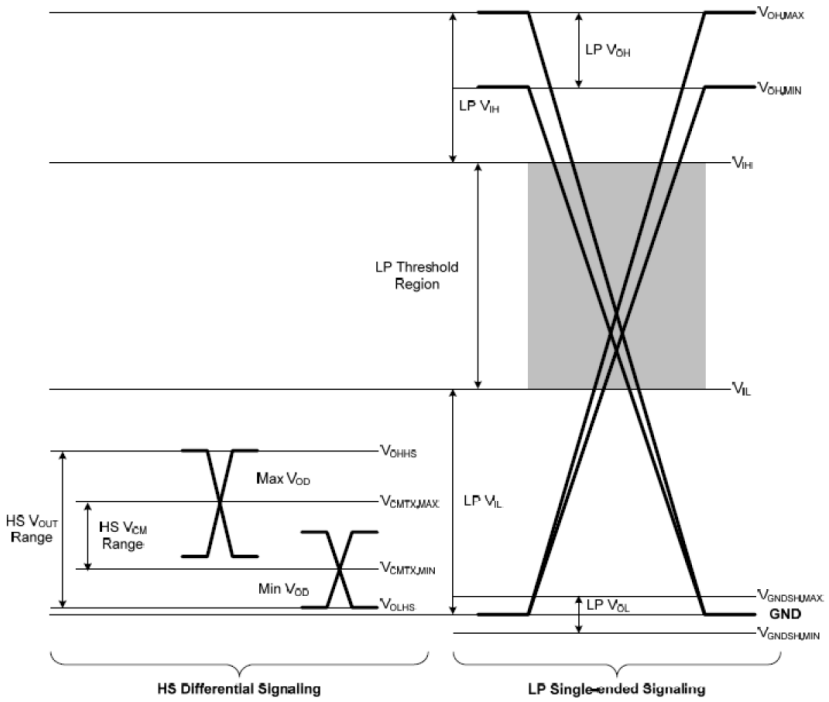


VDD rising time

5.1.2 Signal electrical characteristics

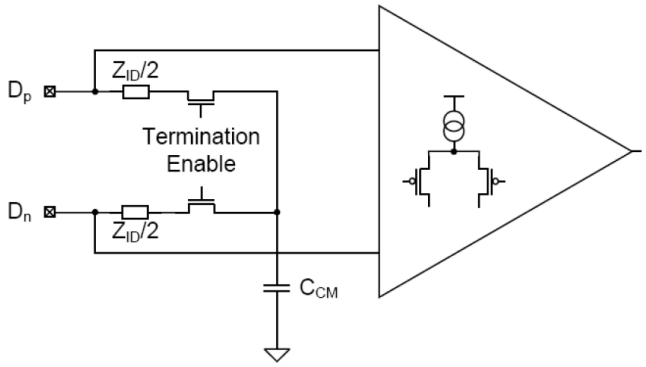
MIPI DC characteristics are as follows:

MIPI Receiver Differential Input (DC Characteristics)					
Symbol	Parameter	Min	Typ	Max	Unit
BR_{MIPI}	Input data bit rate	200	-	1000	Mbps
V_{CMRX}	Common-mode voltage(HS Rx mode)	155	-	330	mV
V_{IDTH}	Differential input high threshold (HS Rx mode)	-	-	70	mV
V_{IDTL}	Differential input low threshold (HS Rx mode)	-70	-	-	mV
$\lvert V_{IDM} \rvert$	Differential input voltage range (HS Rx mode)	70	-	500	mV
V_{IHHS}	Single-end input high voltage (HS Rx mode)	-	-	460	mV
V_{ILHS}	Single-end input low voltage (HS Rx mode)	-40	-	-	mV
Z_{ID}	Differential input impedance	80	100	125	Ω
V_{IHLP}	Logic 1 input voltage (LP Rx mode)	880			mV
V_{ILLP}	Logic 0 input voltage (LP Rx mode)			550	mV



MIPI Receiver Differential Input (AC Characteristics)						
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$\Delta V_{CMRX(HF)}$	Common-mode interference beyond 450MHz		-	-	100	mV
$\Delta V_{CMRX(LF)}$	Common-mode interference 50MHz ~ 450MHz		-50	-	50	mV
C_{CM}	Common-mode termination		-	-	60	pF
UI_{INST}	UI instantaneous		1		12.5	ns

HS RX Scheme

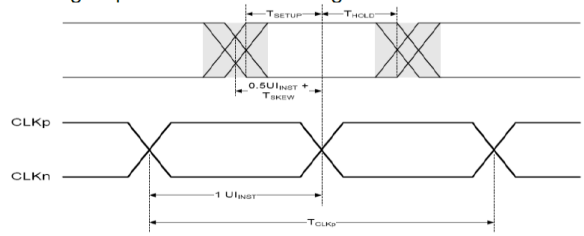


Symbol	Parameter	Min	Typ	Max	Unit	Notes
$T_{SKEW[TX]}$	Data to Clock Skew (mesured at transmitter)	-0.15		0.15	UI_{INST}	1
$T_{SETUP[RX]}$	Data to Clock Setup Time (receiver)	0.25			UI_{INST}	2
$T_{HOLD[RX]}$	Data to Clock Hold Time (receiver)	0.25			UI_{INST}	2

Note:

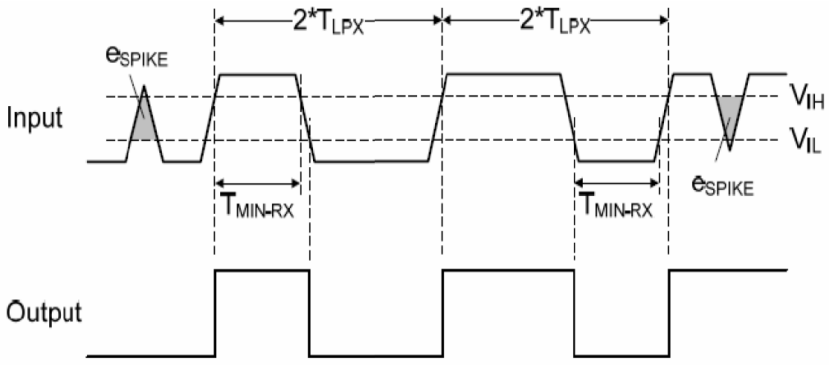
1. Total silicon and package delay budget of 0.25*UI_{INST}
2. Total setup and hold window for receiver of 0.5 *UI_{INST}

MIPI High-Speed Data-clock Timing

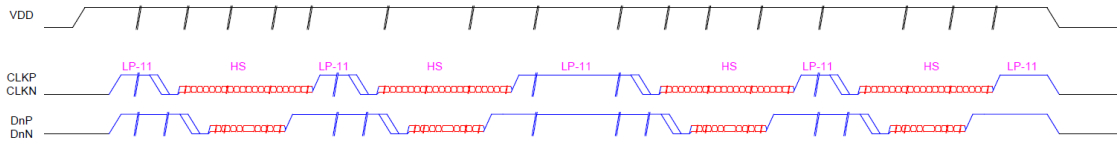


LP Receiver AC Specifications						
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
e_{SPIKE}	Input pulse rejection		-	-	300	V · ps
T_{MIN-RX}	Minimum pulse width response		50	-	-	ns
V_{INT}	Peak interference amplitude		-	-	200	mV
f_{INT}	Interference frequency		450	-	-	MHz

Input Glitch Rejection of Low-Power Receivers



For MIPI data transmission from TX to TCON works properly in video mode, it is suggested that all of MIPI lanes status follow the scheme showed in below. When power is turned on, all lanes (include clock lane) are into LP-11 status first. When TX wants to start transmitting data to TCON, the clock lane is into HS and start toggling. Then data lanes are into HS and data are transmitted. After data transmissions are finished (ex. H-blanking, V-blanking), the data lanes are returned to LP-11, then clock lane, too. The transmission start from LP-11 and stop in LP-11 on all lanes (include clock lane) are the recommended proper operation sequence for MIPI video mode.



The timing definitions are listed in below,

Parameter	Description	Min	Typ	Max	Unit
TCLK-MISS	Timeout for receiver to detect absence of Clock transitions and disable the Clock Lane HS-RX.			60	ns
TCLK-POST	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of THS-TRAIL to the beginning	60 ns + 52*UI			ns

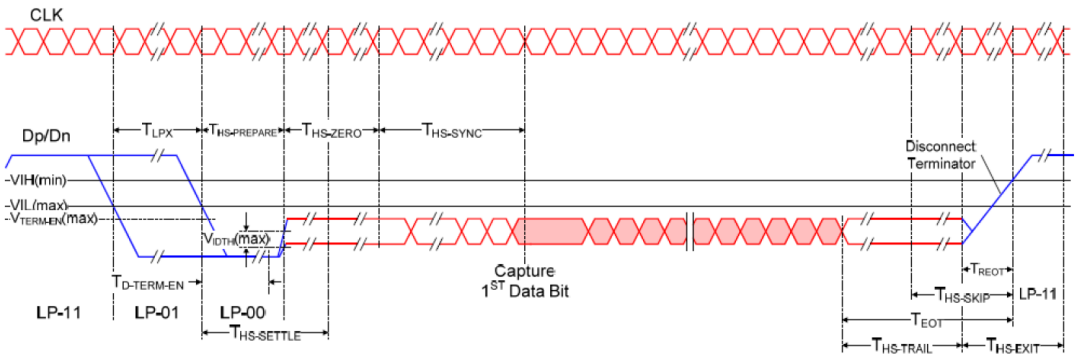
	of TCLK-TRAIL.				
TCLK-PRE	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	8			UI
TCLK-PREPARE	Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission.	38		95	ns
TCLK-SETTLE	Time interval during which the HS receiver shall ignore any Clock Lane HS transitions, starting from the beginning of TCLK-PREPARE.	95		300	ns
TCLK-TERM-EN	Time for the Clock Lane receiver to enable the HS line termination, starting from the time point when Dn crosses VIL,MAX.			38	ns
TCLK-TRAIL	Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst.	60			ns
TCLK-PREPARE + TCLK-ZERO	TCLK-PREPARE + time that the transmitter drives the HS-0 state prior to starting the Clock.	300			ns
TD-TERM-EN	Time for the Data Lane receiver to enable the HS line termination, starting from the time point when Dn crosses VIL,MAX.			35 ns + 4*UI	ns
TEOT	Transmitted time interval from the start of THS-TRAIL or TCLK-TRAIL, to the start of the LP-11 state following a HS burst.			105 ns + 12*UI	ns
THS-EXIT	Time that the transmitter drives LP-11 following a HS burst.	100			ns
THS-SYNC	HS Sync-Sequence '00011101' period		8		UI
THS-PREPARE	Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission	40 ns + 4*UI		85 ns + 6*UI	ns
THS-PREPARE + THS-ZERO	THS-PREPARE + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence.	145 ns + 10*UI			ns

THS-SETTLE	Time interval during which the HS receiver shall ignore any Data Lane HS transitions, starting from the beginning of THS-PREPARE.	85 ns + 6*UI		145 ns + 10*UI	ns
THS-SKIP	Time interval during which the HS-RX should ignore any transitions on the Data Lane, following a HS burst. The end point of the interval is defined as the beginning of the LP-11 state following the HS burst.	40		55 ns + 4*UI	ns
THS-TRAIL	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst	60 ns + 4*UI			ns
TLPX	Transmitted length of any Low-Power state period	50			ns
Ratio TLPX	Ratio of TLPX(MASTER)/TLPX(SLAVE) between Master and Slave side	2/3		3/2	
TTA-GET	Time that the new transmitter drives the Bridge state (LP-00) after accepting control during a Link Turnaround.		5*TLPX		ns
TTA-GO	Time that the transmitter drives the Bridge state (LP-00) before releasing control during a Link Turnaround.		4*TLPX		ns
TTA-SURE	Time that the new transmitter waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround.	TLPX		2*TLPX	ns

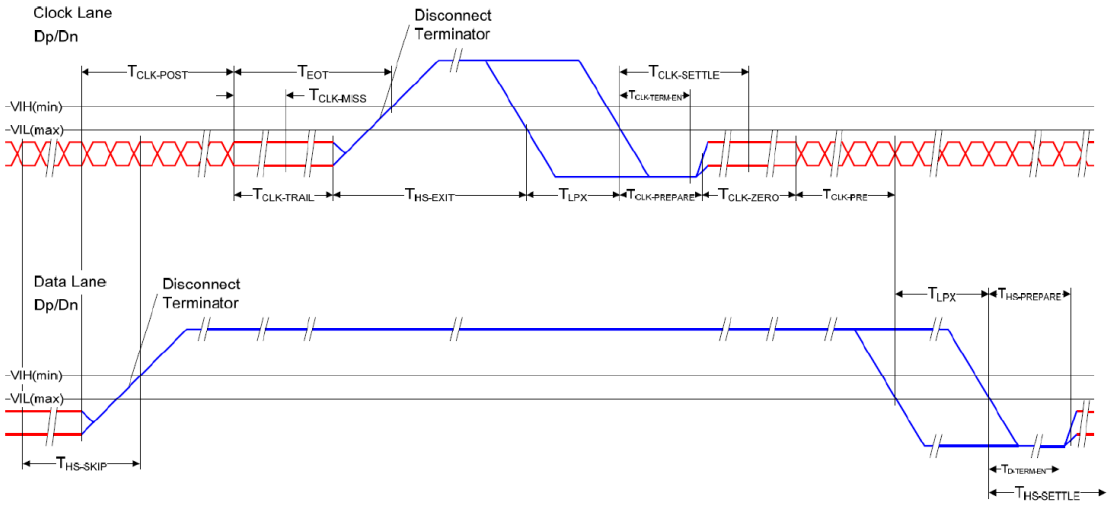
Note:

1. The minimum value depends on the bit rate. Implementations should ensure proper operation for all the supported bit rates.
2. TLPX is an internal state machine timing reference. Externally measured values may differ slightly from the specified values due to asymmetrical rise and fall times.
3. The I-chip of AUO use is not support BTA (BTA define ignore).

High-Speed Data Transmission in Bursts



Switching the Clock Lane between Clock Transmission and Low-Power Mode



Turnaround Procedure

5.2 Backlight unit

Parameter	Min	Typ	Max	Unit	Note
LED voltage (VL)		18		[V]	2
LED current (IL)		240		[mA]	2
LED power (PL)		4.32		[W]	
LED lite time (MTBF)		100,000		[Hour]	1

Note 1: The “LED lift time” is defined as the module brightness decrease to 50% original brightness that the ambient temperature is 25℃ and typical LED Current at 240 mA

Note 2: The variance of LED Light Bar power consumption is ±10%. Calculator value for reference (IL × VL = PLED)

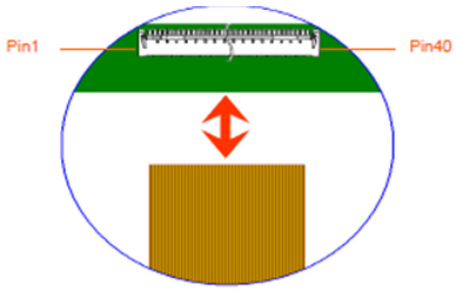
5.3 Interface connector

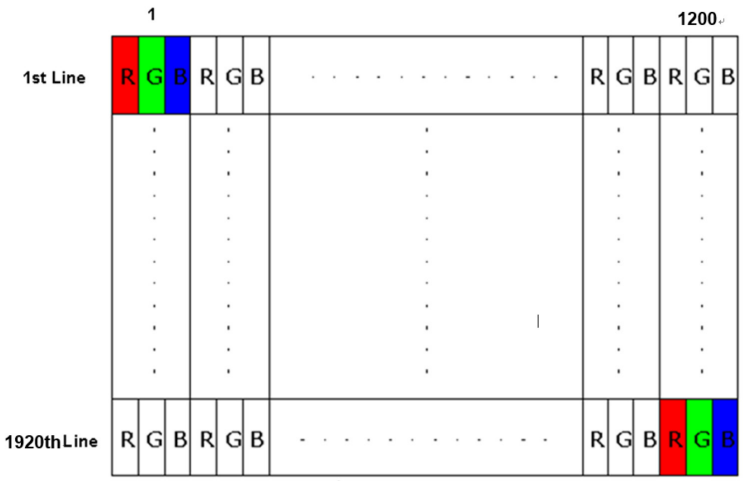
5.3.1 TFT connector(CN1)

Connector Name / Designation	For Signal Connector
Manufacturer	HRS
Type / Part Number	FH34SRJ-40S-0.5SH or compatible
Mating Housing/Part Number	FPC

Pin	Symbol	Description
1	LED+	Anode for light bar
2	LED+	Anode for light bar
3	NC	No connection
4	LED1-	Cathode for light bar
5	LED2-	Cathode for light bar
6	LED3-	Cathode for light bar
7	NC	No connection
8	NC	No connection
9	NC	No connection
10	NC	No connection
11	NC	No connection
12	NC	No connection
13	ID	High
14	VDD	3.3V input power
15	VDD	3.3V input power
16	VDD	3.3V input power
17	NC	No connection
18	REZX	Device reset signal
19	LEDPWM_OUT	PWM control signal for LED driver(CABA)
20	GND	Ground
21	GND	Ground
22	NC	No connection
23	NC	No connection
24	NC	No connection
25	GND	Ground
26	D0+	MIPI differential data 0 input(Positive)

27	D0-	MIPI differential data 0 input(Negative)
28	GND	Ground
29	D1+	MIPI differential data 1 input(Positive)
30	D1-	MIPI differential data 1 input(Negative)
31	GND	Ground
32	CLK+	MIPI differential data CLK input(Positive)
33	CLK-	MIPI differential data CLK input(Negative)
34	GND	Ground
35	D2+	MIPI differential data 2 input(Positive)
36	D2-	MIPI differential data 2 input(Negative)
37	GND	Ground
38	D3+	MIPI differential data 3 input(Positive)
39	D3-	MIPI differential data 3 input(Negative)
40	GND	GND





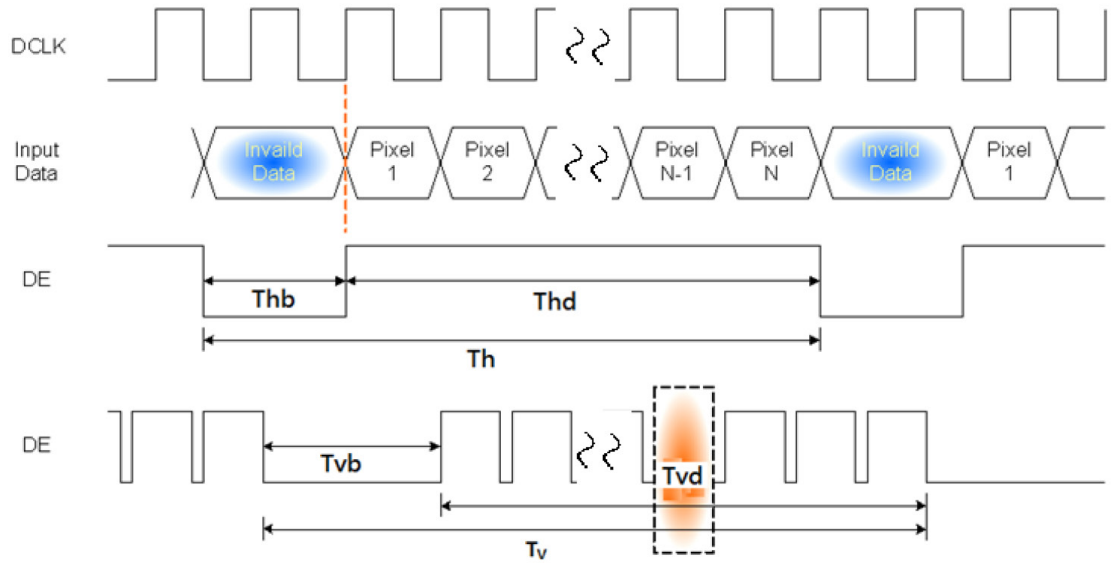
6. Signal characteristics

6.1 Interface timing

6.1.1 Timing characteristics

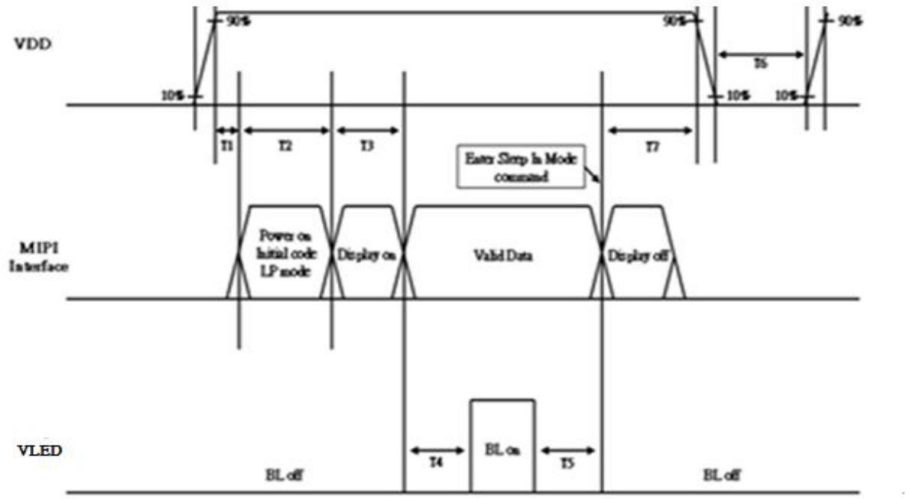
Parameter		Symbol	Min.	Typ.	Max.	Unit
Frame Rate		---	---	60	---	Hz
Clock frequency		1/ T_{Clock}	477	499	500	MHz
Vertical Section	Period	T_v	1981	1981	1982	T_{Line}
	Active	T_{vd}	1920			
	Blanking	T_{vb}	61	61	62	
Horizontal Section	Period	T_h	1275	1341	1342	T_{Clock}
	Active	T_{hd}	1200			
	Blanking	T_{hb}	75	141	142	

6.1.2 Timing diagram



6.2 Power ON/OFF sequence

Power on/off sequence is as follows. Interface signals and LED on/off sequence are also shown in the chart.



6.3 MIPI control

NO	Type	Remark
1	Sleep in/ out	Sleep in:0x10, sleep out:0x11,
2	Display on/off	Display on:0x29 Display off:0x28

7. Reliability Test

Environment test conditions are listed as following table.

Items	Required Condition	Note
Temperature Humidity Bias (THB)	Ta=40℃, 80%RH, 240hours	
High Temperature Operation (HTO)	Ts= 60℃, 240hours	3
Low Temperature Operation (LTO)	Ta= -10℃, 240hours	
High Temperature Storage (HTS)	Ta= 70℃, 240hours	
Low Temperature Storage (LTS)	Ta= -20℃, 240hours	
Thermal Shock Test (TST)	-20℃/30min, 60℃/30min, 100 cycles	
On/Off Test	On/10sec, Off/10sec, 30,000 cycles	
ESD (ElectroStatic Discharge)	Contact Discharge: ± 4KV,	
	Air Discharge: ± 8KV,	

Note 1: The TFT-LCD module will not sustain damage after being subjected to 100 cycles of rapid temperature change. A cycle of rapid temperature change consists of varying the temperature from -10℃ to 50℃, and back again. Power is not applied during the test. After temperature cycling, the unit is placed in normal room ambient for at least 4 hours before power on.

Note 2: According to EN61000-4-2 , ESD class B: Some performance degradation allowed. No data lost. Self-recoverable. No hardware failures.

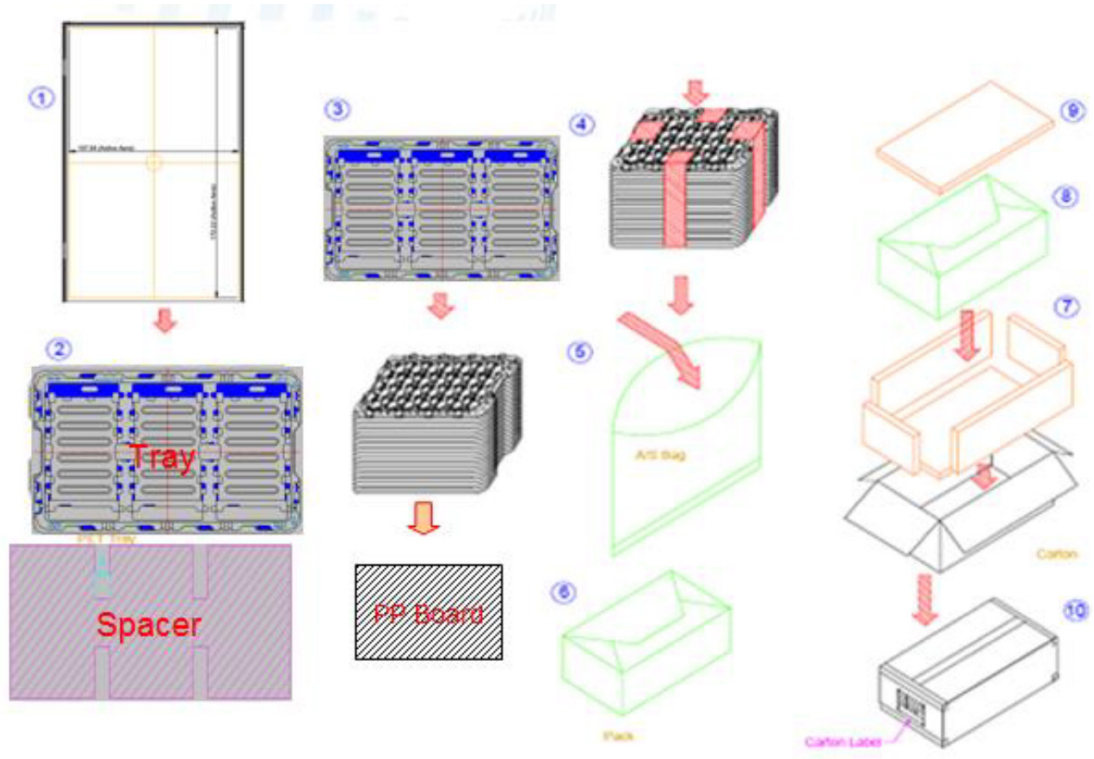
Note 3: TFT surface.

Note 4,In case of malfunction defect caused by ESD damage, if it would be recovered to normal state after resetting, it would be judge as a good part.

Note 5, EL evaluation should be accepted from reliability test with humidity and temperature: Some defects such as black spot/blemish can happen by natural chemical reaction with humidity and Fluorescence EL.

Note 6, Failure Judgment Criterion: Basic Specification Electrical Characteristic, Mechanical Characteristic, Optical Characteristic.

8. Shipping package
(TBD)



6 pcs/tray
(11+1)trays/carton
Total 66 pcs panel/carton
Total carton weight: 10.2 Kg
Carton type: 520*340*250mm
PP Board: Put it on the bottom of the Tray

9. Mechanical Characteristics